Moletronics II

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EXECUTIVE SUMMARY

Molecular Electronics and Quantum Computing present very different challenges in the development of their potential for future information technology. In Molecular Electronics, the challenges revolve around effectively dealing with the potential for a very high density of devices. In Quantum Computing, a fairly small number of actual devices (bits) is needed, but the technical challenges of creating and controlling those devices are extreme.

Molecular Electronics Summary

The field of molecular electronics, defined as the investigation of electronic transport through individual molecules, is one of tremendous intellectual excitement. It is premature to speculate as to where such systems might be useful technologically, because gain at the molecular scale has not been achieved, and because the field is just reaching the point where seriously testing molecules as electronic devices may be feasible. It is, nevertheless, straightforward to show that power-dissipation, bit rates, fan-in/out implementations and the need for gain will not simply scale with size. Exploiting molecular electronics will require understanding the special properties of molecules and developing implementations tailored to those properties.

To expedite the development of molecular electronics, we recommend that both basic research and demonstration studies in molecular electronics be structured to provide standard information needed for evaluation and development of potential technological applications of the field:

1) Systematically confirm the relationship between molecular structure and measured device properties, using correlated experimental and theoretical work.

2) Systematically characterize the contacts between molecular devices and conductors and their impact on achievable device performance, including issues of reproducibility and contact resistance.

3) Couple 1) and 2) to routine characterization of electrical engineering properties, as new devices are proposed and demonstrated. Key issues are:

    a) reproducibility of fabrication and characterization of defect rate in self assembly
    b) switching energy (including consideration of contact effects)
    c) number of switching events to failure, identification of failure modes
    d) switching time constant (including consideration of contact effects)
    e) proposal/evaluation of circuit applications

As the knowledge base concerning molecular device properties improves, development of architectural strategies tailored to demonstrated molecular characteristics may be possible. Hybrid (e.g. interfaced to Si-based electronics or organic electronics) architectures will be necessary unless/ until intrinsic molecular gain-producing devices can be developed. It is not clear that useful high performance computational devices can be prepared if CMOS must be used to provide gain. However, such integrated systems may be valuable in developing applications that exploit unique molecular properties (e.g. interfaces to biological or chemical sensing systems, or as inexpensive/flexible application-specific integrated circuits.

Quantum Computing Summary

Over the past six years, important "proof-of-principle" advances have been made in quantum computing. However, even if quantum information science is advancing rapidly, it is far from clear what (if any) will be the near-term impact beyond basic science. There is still no general understanding of the power of quantum versus classical computation (i.e., what is the set of problems for which quantum computers have an in-principle advantage, e.g., in terms of computational complexity?). Moreover, in the case of Shor's algorithm, for which such an advantage has been shown to exist, there is no physical system that has been shown to be suitable for the implementation of large-scale quantum computation.

In view of these considerable uncertainties, we recommend that DARPA develop a broad-based strategy directed to exploring the space of potential applications of quantum computing and to assessing the suitability of diverse physical systems for quantum information processing. Hand in hand with these activities should proceed investigations of computer architectures that could most effectively bridge the gap from algorithm to physical implementation.

More specifically, we recommend the following areas of emphasis.

1. Algorithms – It is extremely important to delineate the domains for which quantum information processing offers unique advantages over classical computation. This largely theoretical program should be broadly defined, and should include, for example, computer scientists, theoretical physicists, control and process engineers. Recall that one of the few examples for which quantum computation offers an exponential win over classical computation is simulating quantum evolution by a quantum computer, which may ultimately be important for the development of quantum technologies.

2. Error correction and fault tolerance – It should be emphasized that there is a wide gulf between the abstract fault tolerant architectures for a quantum computer and physical implementations currently being pursued. Serious effort is needed to address the open question of how to accomplish all of the requisite interactions and read outs in a given physical system.

3. Physical implementations – There is no credible capability (either theoretically or experimentally) for the realization of large-scale quantum computation. It is altogether too early to suggest focusing on any particular system(s) as representing the "best path(s)" toward large-scale implementations. Experiments to isolate and control individual quantum systems, emphasizing issues of "quantum wiring" (how physical interactions between qubits lead to actual networks), as well as input/output (how to initialize and readout networks of qubits) should be emphasized. An example of a system without suitable scaling properties is so-called ensemble quantum computing via NMR.

4. Quantum communication – We did not study in detail quantum cryptography. However, this is area of importance for DOD, as well as the wider community, that likely will have shorter term impact than will quantum computing. Demonstrations to date with weak coherent pulses are useful, but do not yet achieve secure communications. A number of critical technical advances are required to achieve this important goal.

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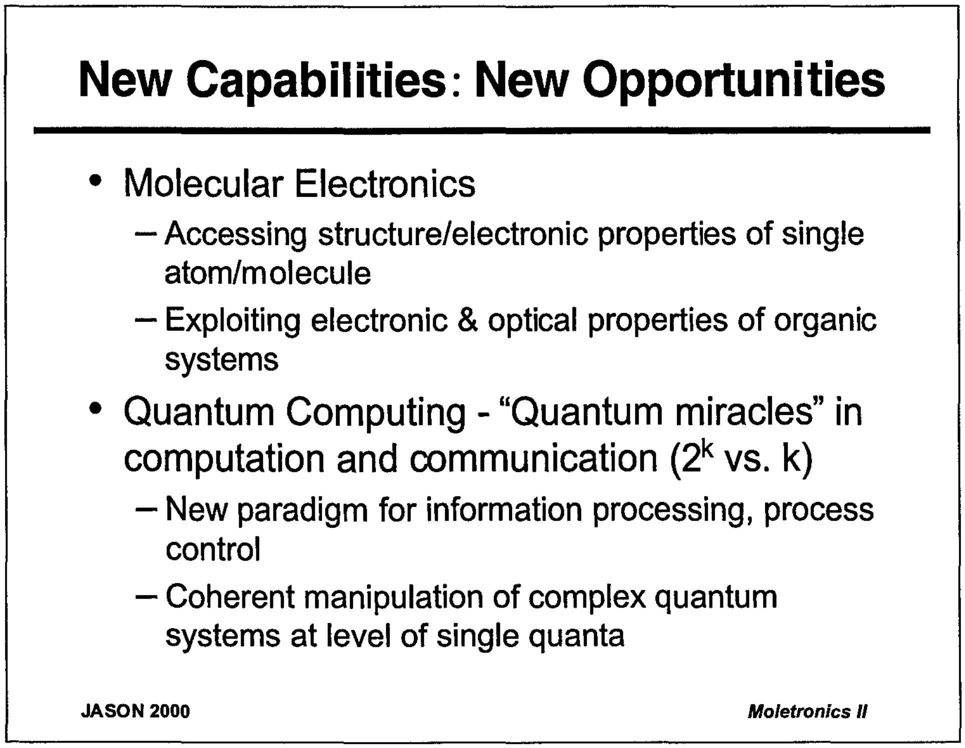

New Capabilities: New Opportunities

- Molecular Electronics
  - Accessing structure/electronic properties of single atom/molecule
  - Exploiting electronic & optical properties of organic systems
- Quantum Computing - "Quantum miracles" in computation and communication (2^k vs. k)
  - New paradigm for information processing, process control
  - Coherent manipulation of complex quantum systems at level of single quanta

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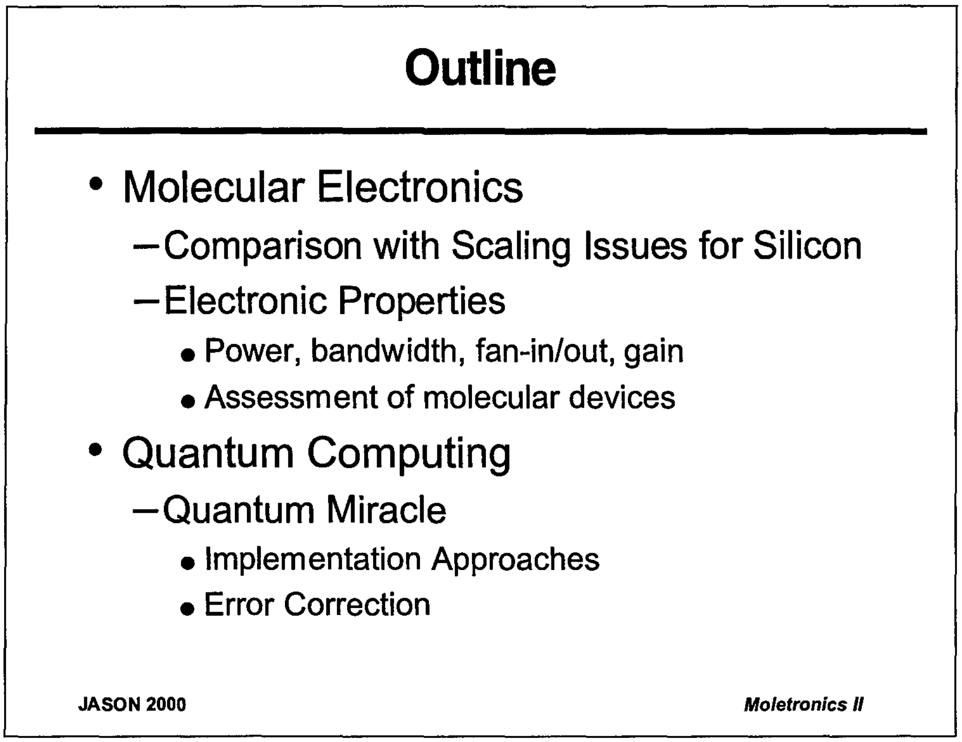
I. INTRODUCTION

The charge for this JASON study was to evaluate several technical issues associated with the development of electronic devices based on molecular and quantum systems. One program in this area, designated as Moletronics, is focused on the construction and exploitation of molecular-scale electronic devices for computational purposes. The focus on molecular systems is spurred by the belief that within 10-20 years, fundamental limitations will be imposed by the use of crystalline semiconductors in current Si-based VLSI approaches to electronic device fabrication. Due to these fundamental limitations, the empirical relationship that describes yearly improvements in computational power (Moore's Law) will cease to describe the rate of progress. The hope is that development of the capability to perform computational processes using devices fabricated on the molecular scale will enable further increases in computational performance to be sustained.

One of the key concerns posed to the JASONs was how one would efficiently address molecular-scale devices even if such could be made. Significant spatial overhead arising from the areal demands of interconnects affects current general purpose chip designs, and this problem will become exacerbated as the device density increases. The construction of well-behaved molecular-scale computational logic devices would not necessarily be of practical interest if the devices could not be addressed in a fashion that would retain the high density or other advantages characteristic of molecules.



Outline

- Molecular Electronics
  - –Comparison with Scaling Issues for Silicon
  - –Electronic Properties
    - Power, bandwidth, fan-in/out, gain
    - Assessment of molecular devices
- Quantum Computing
  - –Quantum Miracle
    - Implementation Approaches
    - Error Correction

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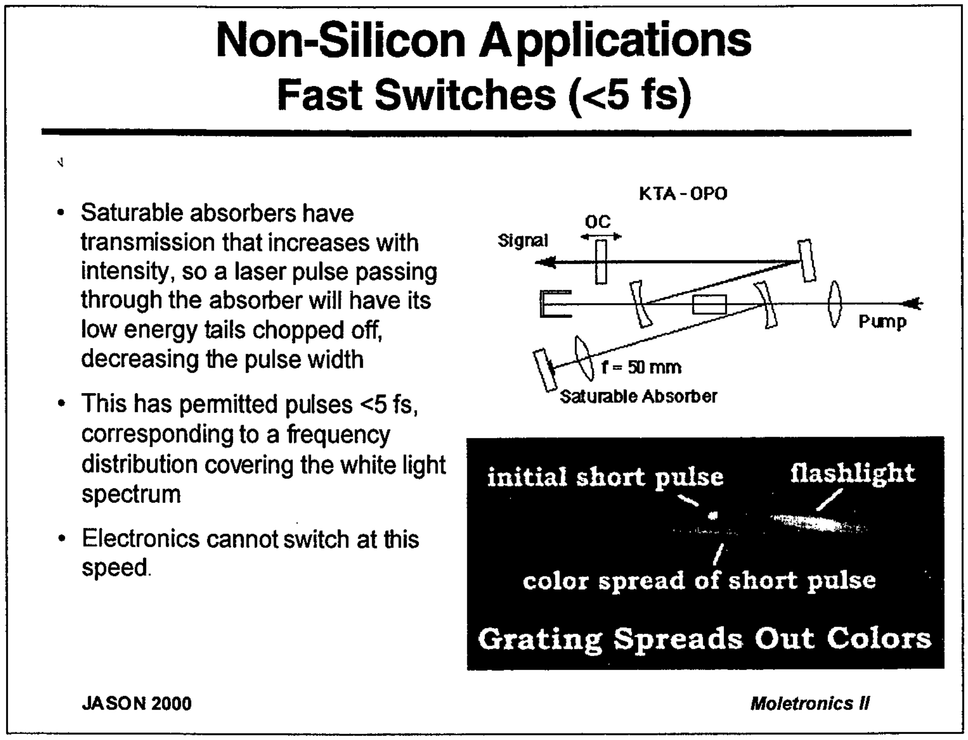
I. Introduction (cont'd)

To effectively address this question, the JASONs needed to evaluate the current state-of-the-art in molecular-scale electronic devices. The current performance characteristics will set some boundaries on the types of device functions that have been accomplished and additionally will frame the types of devices that can be envisioned, how such devices might be addressed, and what types of architectures might be used. This JASON study therefore attempted to address key milestones and outstanding research issues on the single molecular electronic device scale which must be defined before appropriate questions concerning the interconnect/architecture scale can even be formulated. The goal was to identify bottlenecks that will be faced when attempting to transition current research on single molecular-scale electronic devices into macroscopically addressable, potentially useful, computational schemes and systems.

A second, and quite different, program in future computational possibilities is Quantum Computation. Quantum computation represents a new paradigm for information processing and process control. The enabling concept of quantum computing involves the coherent manipulation of complex quantum systems at the level of single quanta, performing a computation in an entangled state, and reading out the answer from an observation of the final stage of the entangled observable as the final step of the computational process. The JASONs were specifically asked to evaluate and address the input/output issues associated with information flow involved in interfacing a quantum computer to the macroscopic world. Because the issues are technically so different from those of molecular-electronic devices (assumed to be operating as classical computational processes for our purposes), the results of this portion of the study are presented in a separate section (Section III) of this report.



Non-Silicon Applications
Fast Switches (<5 fs)

- Saturable absorbers have transmission that increases with intensity, so a laser pulse passing through the absorber will have its low energy tails chopped off, decreasing the pulse width
- This has permitted pulses <5 fs, corresponding to a frequency distribution covering the white light spectrum
- Electronics cannot switch at this speed.

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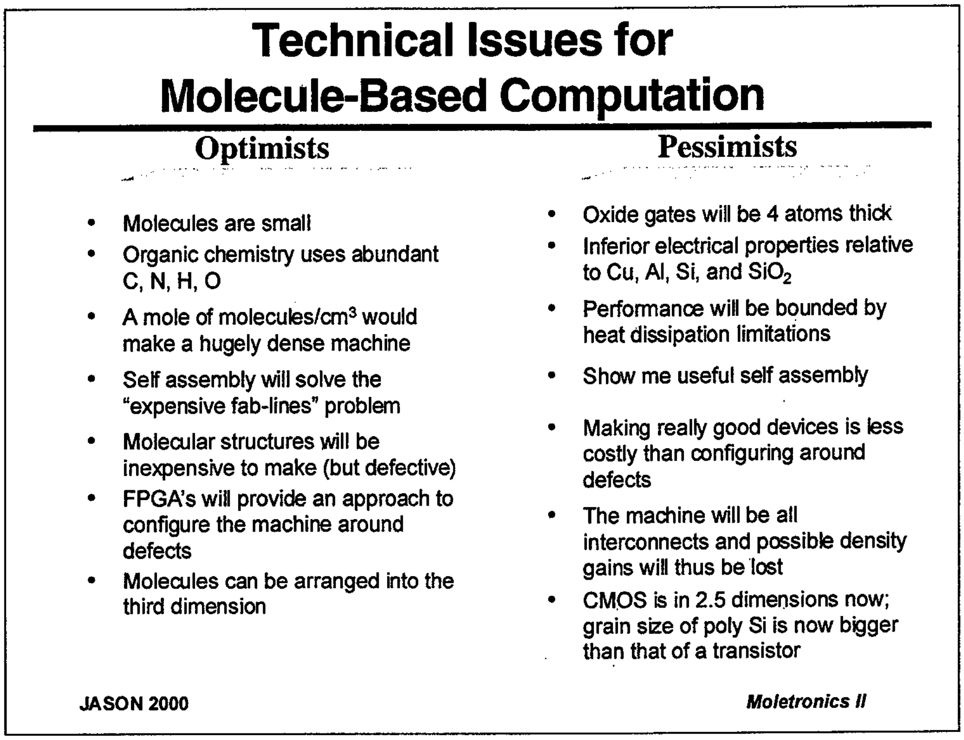
II. MOLECULAR ELECTRONICS

Molecular electronics has been popularly represented as a one-to-one replacement for Si-based microelectronics. Before proceeding to our technical discussion of this possibility, we first note that alternative perspectives are likely to be valuable.

II.A Analog Molecular Electronics

There may be important applications for which molecular devices are much better than silicon. An example is fast optical shutters. Saturable absorbers are molecules whose transparency depends on the intensity of light incident on the absorber: increasing intensity increases transparency. At slow speeds, optical device modulation is done using conventional electronics. However molecules change their transparency very rapidly and can be used as fast optical switches to create very short optical pulse trains. This absorber system is in fact an example of a sensor/actuator combination in which the molecular properties naturally change to produce the appropriate response to some detected signal. Such systems would be very difficult or impossible to implement in Si. Molecules can be thus considered high speed replacements for electronics where their natural properties accomplish a task in one step that requires many steps when implemented using traditional electronics.

In addition, molecules or molecular assemblies designed for appropriate analog electronic response could be used to interface sensors to silicon integrated circuits. The molecules would then serve dual functinality, acting as a (possibly self assembling) link to the silicon, and also acting as a pre-processor or amplifier for the transfer of information.



Technical Issues for Molecule-Based Computation

Optimists	Pessimists
Molecules are small	Oxide gates will be 4 atoms thick
Organic chemistry uses abundant C, N, H, O	Inferior electrical properties relative to Cu, Al, Si, and SiO_2
A mole of molecules/cm^3 would make a hugely dense machine	Performance will be bounded by heat dissipation limitations
Self assembly will solve the "expensive fab-lines" problem	Show me useful self assembly
Molecular structures will be inexpensive to make (but defective)	Making really good devices is less costly than configuring around defects
FPGA's will provide an approach to configure the machine around defects	The machine will be all interconnects and possible density gains will thus be lost
Molecules can be arranged into the third dimension	CMOS is in 2.5 dimensions now; grain size of poly Si is now bigger than that of a transistor

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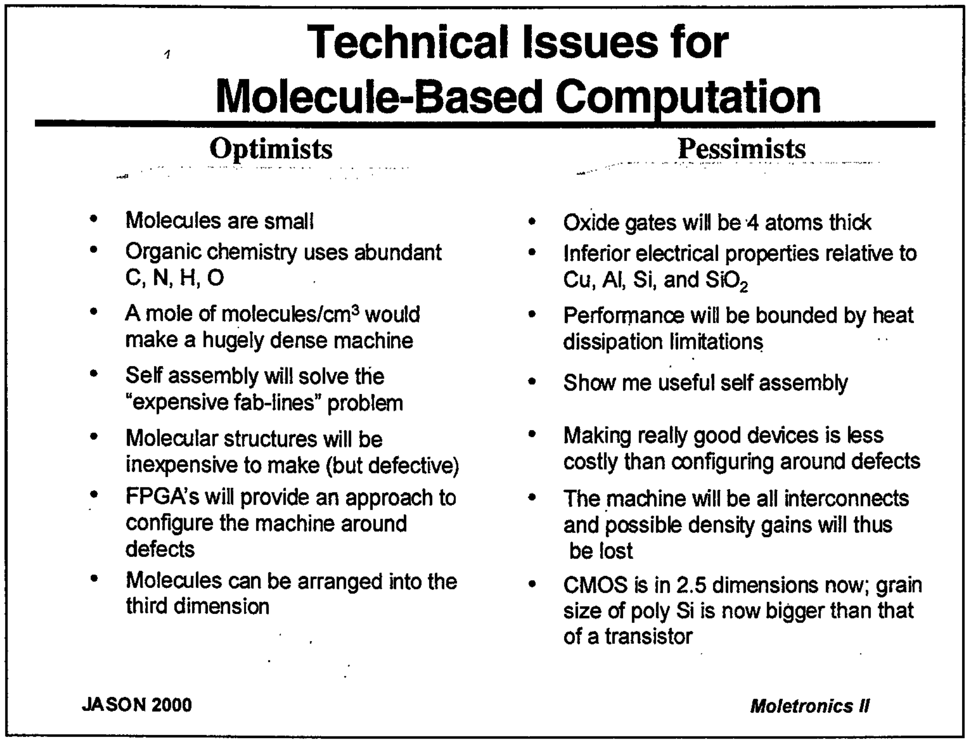
II.B Technical Issues for Molecule-Based Computation

Molecular- based computation must compete with Si-based computation. Before embarking on a detailed technical evaluation of where technical advantage may lie, it is useful to frame the key technical issues that will be involved with implementation of a molecular electronic computa-tional system. These issues can be usefully framed in terms of a point/counterpoint set of statements. Such statements can be divided into two categories: those that are optimistic (o) about the future of molecular electronic devices, and conversely those that are pessimistic (p) about the prospects for constructing a useful molecular-scale computational computing system. These issues form a good basis for discussion of the various technical aspects of concern that form the remainder of the report.

1. o) Molecules are small: therefore the device density is certain to be high.

   p) The semiconductor industry roadmap projects that gate oxides on Si transistors will be 4 atoms thick in 10-15 years. The gate length and width perhaps cannot be scaled down in accord with the gate oxide thickness, but this is not certain either. Further-more, tunneling effects will be exacerbated if organic materials, as opposed to inorganic oxides, are used to provide the functions in molecular devices.

2. o) Organic chemistry uses the abundant elements C, H, O and N, in molecules that can be fabricated to achieve desired structure/function relationships using the powerful methodology of organic synthesis, in a fashion that cannot be matched by the



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II.B Technical Issues for Molecule-Based Computation (cont'd)

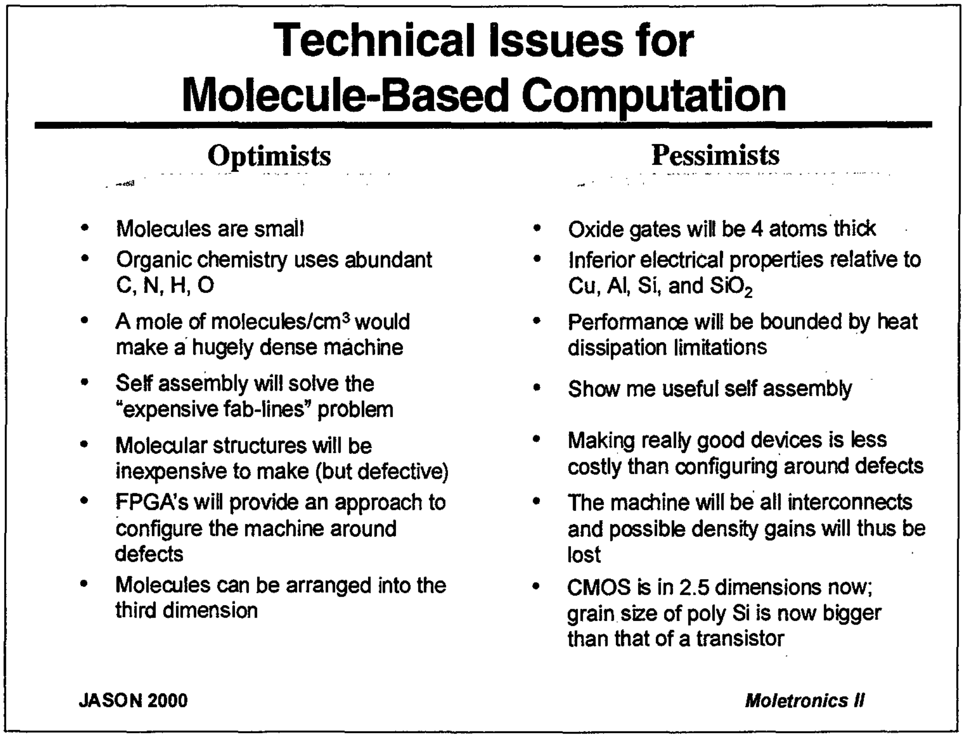
solid state materials growth processes that are used to make Si, GaAs, InP, and other inorganic solids.

p) Organic compounds in general have inferior electrical properties to those currently used in electronic devices. No organic material is as conductive as Au or Cu nor as insulating as SiO_2 or Al_2O_3. No organic compounds have charge carrier mobilities that approach the mobilites of carriers in lattices with periodic potentials such as crystalline Si. Devices made from such electrically-inferior starting materials must therefore necessarily be more dissipative, less rectifying, and show poorer electrical device properties, than ones made using the materials employed in current VLSI technology.

3. o) If molecules could form individual electronic devices, a 1 cm^3 volume could contain perhaps 10^{20} electrical devices.

   p) Heat dissipation limitations on a macroscopic device will severely restrict the rate (and thus the clock speed) at which such devices can be operated and read out.

4. o) Self-assembly methods will allow assembly of complex structures on the 100 nm scale that will allow fabrication of "nanoblocks", which can, in turn, be themselves addressed with interconnects to mate with larger-scale VLSI technology.



Technical Issues for Molecule-Based Computation

Optimists	Pessimists
• Molecules are small	• Oxide gates will be 4 atoms thick
• Organic chemistry uses abundant C, N, H, O	• Inferior electrical properties relative to Cu, Al, Si, and SiO_2
• A mole of molecules/cm^3 would make a hugely dense machine	• Performance will be bounded by heat dissipation limitations
• Self assembly will solve the "expensive fab-lines" problem	• Show me useful self assembly
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• Molecules can be arranged into the third dimension	• CMOS is in 2.5 dimensions now; grain size of poly Si is now bigger than that of a transistor

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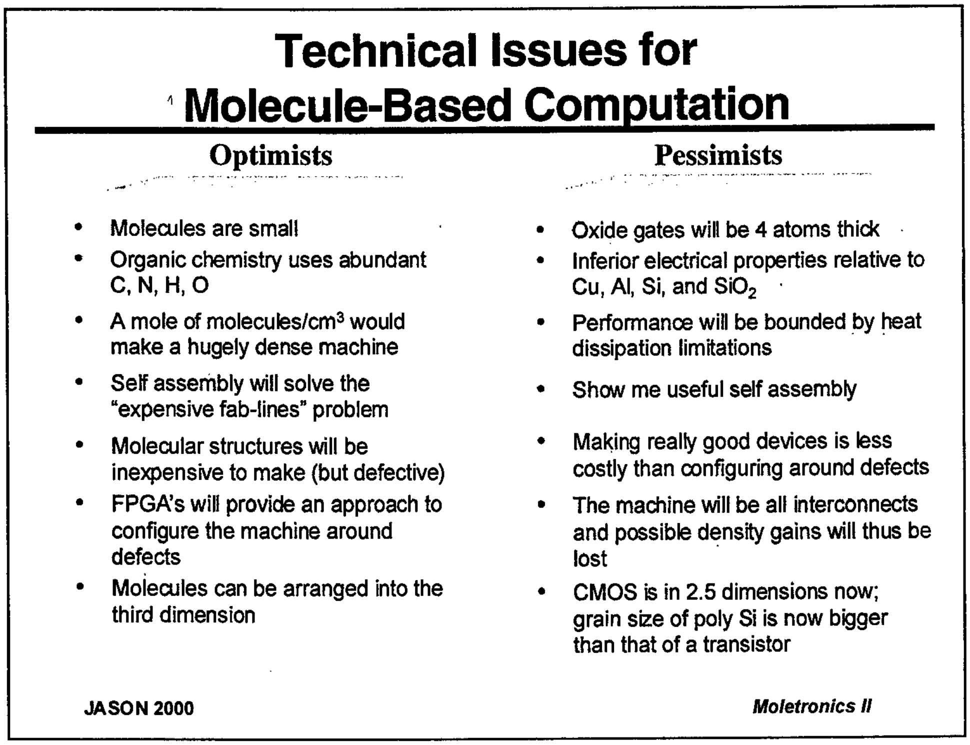
II.B Technical Issues for Molecule-Based Computation (cont'd)

p) A research/technology breakthrough is needed in order to obtain such a multiplexing capability without being limited by the density of the CMOS addressing amplifiers.

5. o) Molecular structures will be inexpensive to make, but they will likely be defective and thus will require programming around defects.

p) Modern industry is already addressing this issue. A tremendous premium is paid in conventional semiconductor fabrication processes to obtain low defect levels. If it were economical to tolerate higher defect levels and to accommodate the presence of such with fault-tolerant software, the free market would likely have already implemented this approach. The tradeoffs involved are already well-known from computational theory and its applications; above a certain level of defects, it is just too hard and too expensive to correct for defects, especially if the defects are in different locations on each device.

6. o) Commercial field programmable gate arrays (FPGA's) provide an approach that is already being implemented, in which one can flexibly configure a machine to route around defective resources and which provides a general computing capability. One simply needs to implement this approach for molecular devices as well.



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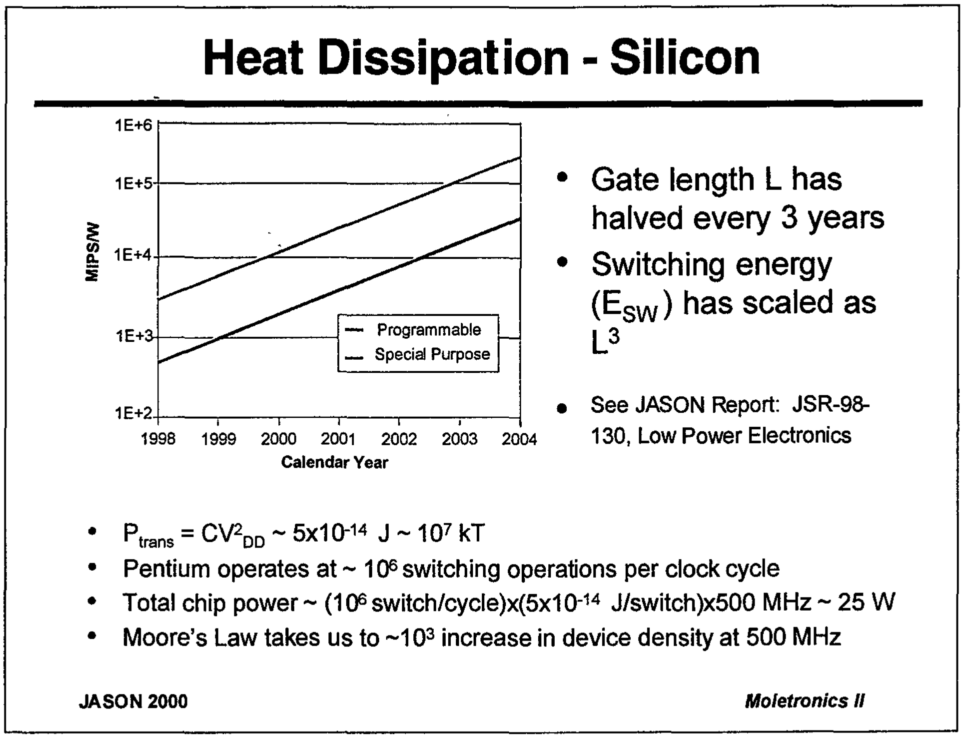
II.B Technical Issues for Molecule-Based Computation (cont'd)

p) To obtain flexibility to route around defects, FPGA's operate at much reduced density relative to special purpose hardware configurations. Most look up tables in FPGA's merely serve as interconnects. Such machines generally have significant latency compared to what could be done with a special purpose machine, and also consume more power than a special purpose processor would. Routing around defects that are not stable with time, or configuring a defective machine with defective resources, is not inexpensive nor easy to envision implementing in practice.

7. o) Molecular devices will have an advantage over VLSI methods in that molecules can be designed to self-assemble into three dimensional structures, whereas current VLSI methods are primarily 2-dimensional in nature.

p) The grain size of polycrystalline Si is now bigger than that of a transistor, so Si will likely be assembled into three dimensions in the future as well.

The above comments admittedly represent extreme view-points, but they serve to illustrate the dichotomy in both outlook and technical analysis that needs to be considered, and reconciled, prior to formulating a rational approach to the development and exploitation of a useful computing technology based on molecular electronics.



Heat Dissipation - Silicon

- Gate length L has halved every 3 years
- Switching energy (E_{SW}) has scaled as L^3
- See JASON Report: JSR-98-130, Low Power Electronics

- $P_{trans} = CV^2_{DD} \sim 5\text{x}10^{-14}$ J ~ 10^7 kT
- Pentium operates at ~ 10^6 switching operations per clock cycle
- Total chip power ~ (10^6 switch/cycle)x($5\text{x}10^{-14}$ J/switch)x500 MHz ~ 25 W
- Moore's Law takes us to ~10^3 increase in device density at 500 MHz

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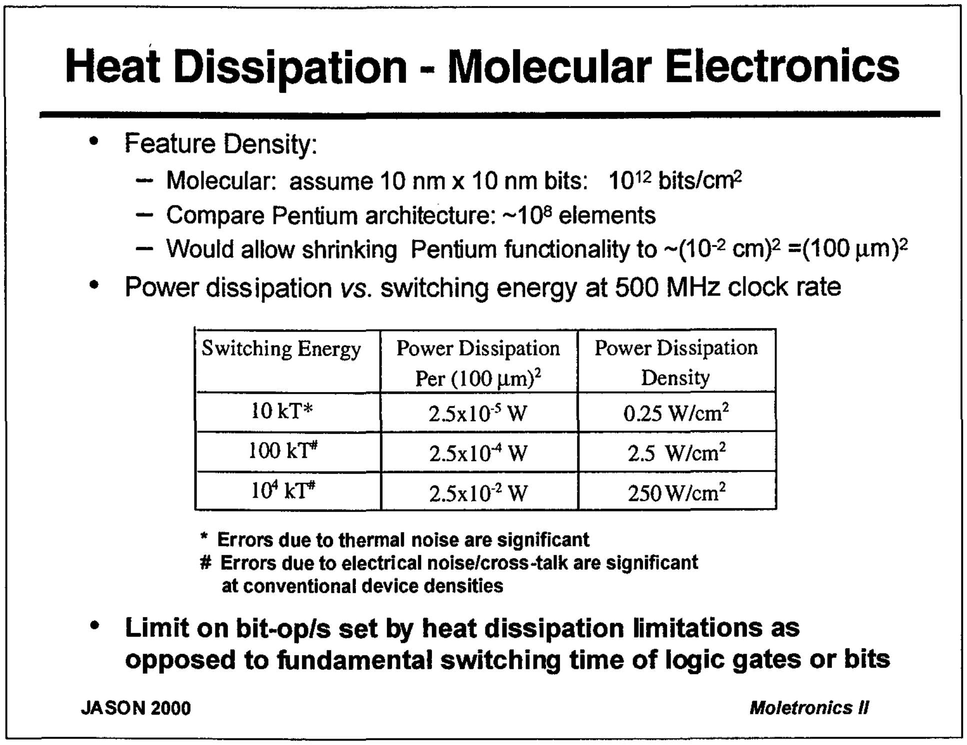
II.B.1 Power Issues

II.B.1.a Heat dissipation

Scaling of integrated circuits to increasing densities has been possible because the switching energy has decreased roughly as the cube of the device size, leading to modern devices that operate at switching energies as small as 10^6 kT. Such scaling of the switching energy with size cannot continue indefinitely, with ultimate limits defined by noise issues as discussed in Appendix A.

Switching energy alone, of course, does not represent the total power consumption even in arithmetic operations, because most of the power consumption is associated with other tasks, especially moving the data. In typical processors (e.g. the Pentium), arithmetic may consume only 10% of the total power. Power consumption is thus heavily dependent on the specific architecture of the processor, but can be described in terms of an effective number of switching events per clock cycle (~10^6 for the Pentium).

No estimate is yet available for the partition of energy consumption between arithmetic and information flow in a molecular computer. As will be discussed later in this report, credible predictions of such properties cannot be made until a serious evaluation of the device properties of the components of a molecular electronics-based computational machine is available.



Heat Dissipation - Molecular Electronics

- Feature Density:
  - Molecular: assume 10 nm x 10 nm bits: 10^{12} bits/cm^2
  - Compare Pentium architecture: ~10^8 elements
  - Would allow shrinking Pentium functionality to ~$(10^{-2}\ \text{cm})^2 = (100\ \mu\text{m})^2$
- Power dissipation *vs.* switching energy at 500 MHz clock rate

Switching Energy	Power Dissipation Per (100 μm)^2	Power Dissipation Density
10 kT*	$2.5\text{x}10^{-5}$ W	0.25 W/cm^2
100 kT#	$2.5\text{x}10^{-4}$ W	2.5 W/cm^2
10^4 kT#	$2.5\text{x}10^{-2}$ W	250 W/cm^2

*** Errors due to thermal noise are significant**
 # Errors due to electrical noise/cross-talk are significant at conventional device densities

- **Limit on bit-op/s set by heat dissipation limitations as opposed to fundamental switching time of logic gates or bits**

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II.B.1 Power Issues (cont'd)

It has been suggested that molecular electronics-based integrated circuits would obtain their greatest benefits over Si-based electronics because self assembly may allow a fully three-dimensional configuration. Power dissipation in such a case would become a much more serious problem than in two dimensions, because heat sinking depends on contact area.

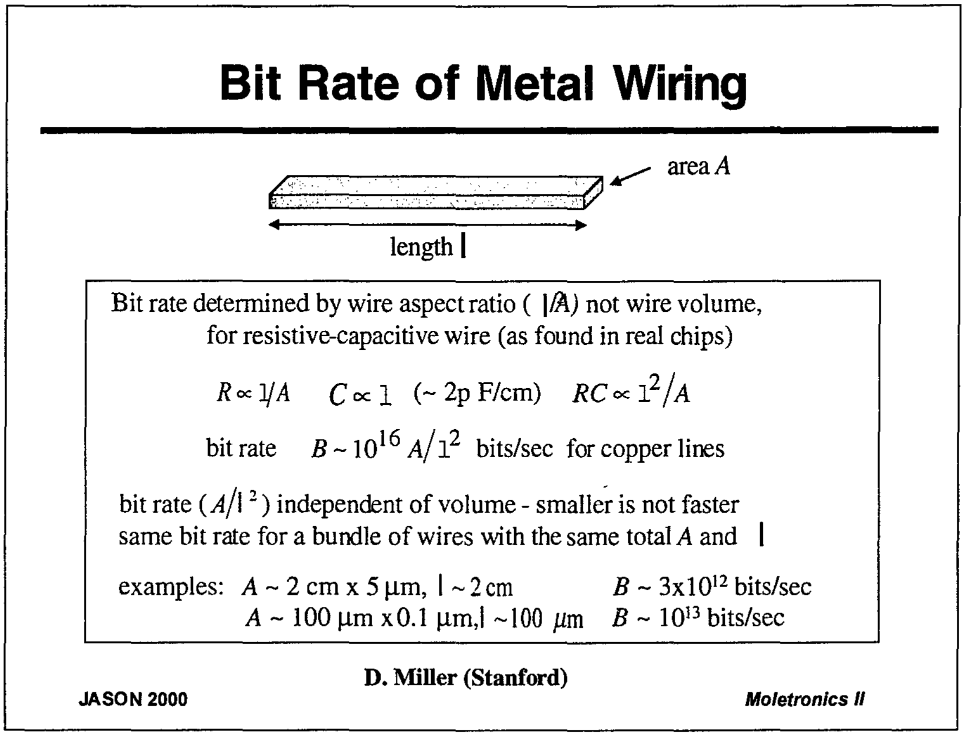
To illustrate the problems of power dissipation that will arise in shrinking computation to molecular electronic feature densities, we simply consider the effects of shrinking a full Pentium IC to the size scale (100 μm)^2 suggested by reasonable molecular electronics device feature sizes. At switching energies (10^4 kT) required to limit errors due to electrical noise, the bulk power dissipation becomes prohibitive at a clock rate of 500 MHz.

Thus, operation of molecular electronics circuitry will require some compromises in performance (in comparison with the silicon baseline), such as :

a) operate at very low switching energies (not yet demonstrated) and accept a non-negligible error rate;

b) disperse molecular electronics circuitry in small clusters separated by a cooling medium (thus sacrificing density);

c) design special-purpose processors for which operation at lower clock speeds is acceptable.



Bit Rate of Metal Wiring

Bit rate determined by wire aspect ratio (l/A) not wire volume,
for resistive-capacitive wire (as found in real chips)

$R \propto 1/A \quad C \propto l$ (~ 2p F/cm) $RC \propto l^2/A$

bit rate $B \sim 10^{16} A/l^2$ bits/sec for copper lines

bit rate (A/l^2) independent of volume - smaller is not faster
same bit rate for a bundle of wires with the same total A and l

examples: $A \sim 2$ cm x 5 µm, $l \sim 2$ cm $B \sim 3\mathrm{x}10^{12}$ bits/sec
$A \sim 100$ µm x 0.1 µm, $l \sim 100$ µm $B \sim 10^{13}$ bits/sec

D. Miller (Stanford)

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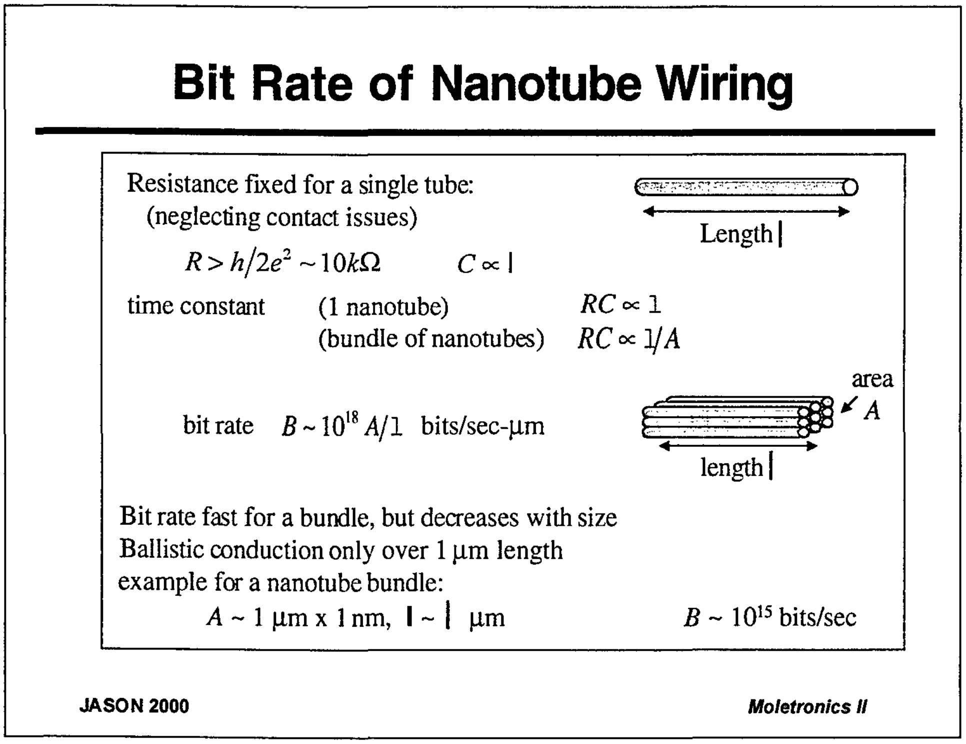
II.B.1.b Information flow

An additional issue relates to the input/output bandwidth of very high device density machines. To illustrate the physical limtations on bit rates of information flow using electrical signals, it is instructive to consider the properties of real metal wires. A high device density molecular electronic computer will essentially be comprised essentially of all interconnects. The ultimate bit rate into and through the machine will therefore be bounded by the bit rate that can be supported by the wiring.

The bit rate for metal wires found in VLSI chips is determined by the resistive-capacitive time constant, *RC,* which is proportional to l^2/A, where *A* is the cross sectional area and *l* is the length as shown above. The bit rate for copper lines is B~10^{16} A/l^2 bit sec^{-1}. Note that this bit rate is the same for a bundle of wires and for a single wire having the same total *A* and *l.* A block of pure copper, 5 µm high, 2 cm wide and 2 cm long, can support a bit rate B~$3\mathrm{x}10^{12}$ bits sec^{-1}.

The bit rate for metal wiring, B~10^{16} A/l^2, remains constant if all three dimensions of the wire are reduced by the same factor. Thus circuits made from smaller dimension wires are not faster, establishing bandwidth limitations on high device density molecular electronic computers.



Bit Rate of Nanotube Wiring

Resistance fixed for a single tube:
(neglecting contact issues)

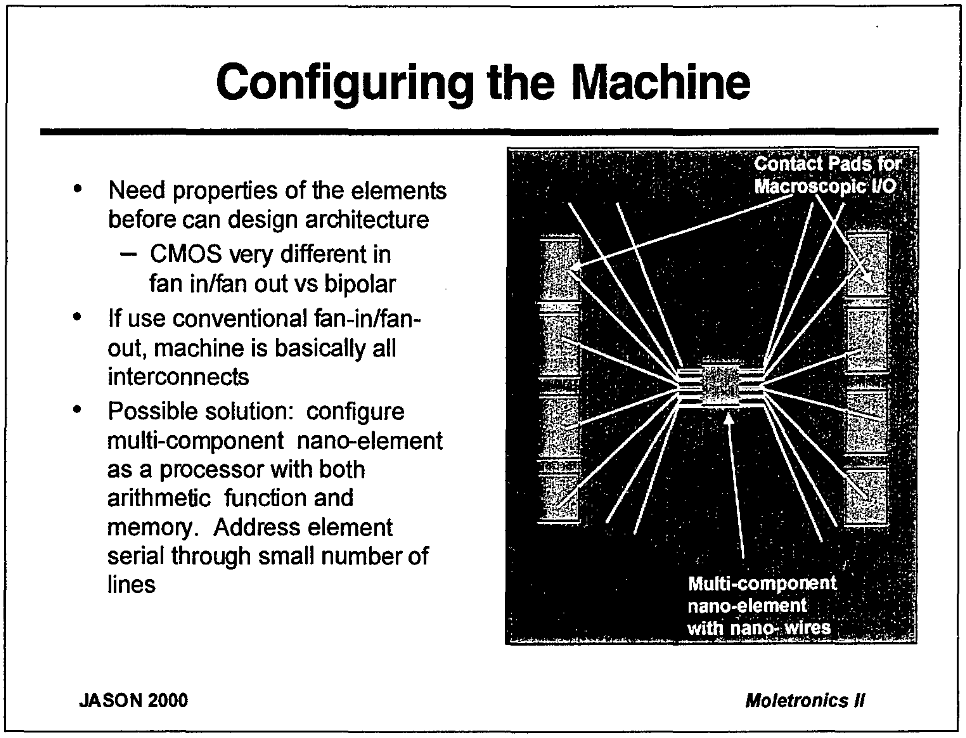
$R > h/2e^2 \sim 10k\Omega$ $C \propto l$

time constant (1 nanotube) $RC \propto 1$
(bundle of nanotubes) $RC \propto 1/A$

bit rate $B \sim 10^{18} A/1$ bits/sec-µm

Bit rate fast for a bundle, but decreases with size
Ballistic conduction only over 1 µm length
example for a nanotube bundle:
$A \sim 1$ µm x 1 nm, l ~ l µm $B \sim 10^{15}$ bits/sec

A possible improvement in bit rate could be obtained if wiring exhibiting quantized conductance, such as carbon nanotubes were used. An ideal nanotube would have a total resistance $R \sim h/2\, e^2 \sim 10\text{k}\Omega$ independent of its length *l*. Since the capacitance C is proportional to *l*, the charging time $RC \propto l$ for a single tube, or $RC \propto l/A$ for a bundle of tubes, decreases with overall size. For a single metallic carbon nanotube 1 µm long, the charging time is therefore $RC \sim 1$ psec. However, contacts from metals to nanotubes are not well understood. As the contact resistance increases above the ideal value, the total resistance increases, and the bit rate decreases. For the typical total observed resistance R ~ 10 MΩ, the time increases to $RC \sim 1$ nsec for a 1 µm length nanotube.



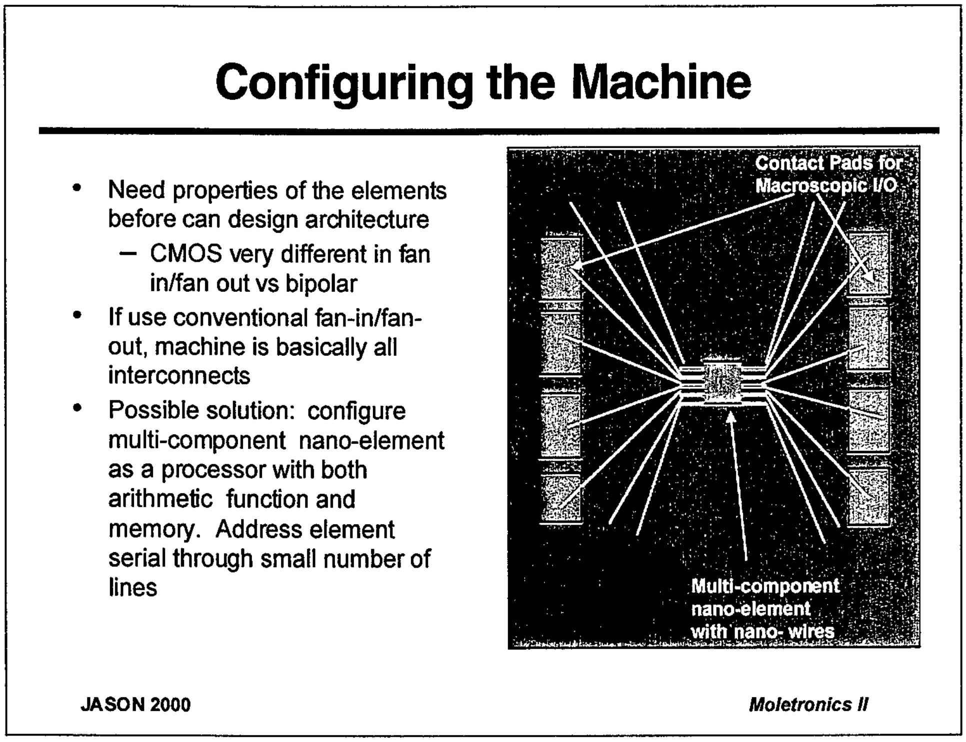
Configuring the Machine

- Need properties of the elements before can design architecture
  - CMOS very different in fan in/fan out vs bipolar
- If use conventional fan-in/fan-out, machine is basically all interconnects
- Possible solution: configure multi-component nano-element as a processor with both arithmetic function and memory. Address element serial through small number of lines

II.B.1.c Fan out

We now turn to issues related to interfacing molecular scale devices with macroscale-sized contacts and input/output connections. It does not take much imagination to realize that connecting 10^{18} nanometer-size objects to the outside world will create serious interfacing problems. At some point, lithographic structures, with minimum linewidths, w, on the order of 100 nm, must provide the input/output (I/O) pathway for the nano scale devices.

For specificity, assume a "nanoblock", i.e. a tileable structure for computation/storage, in the crossbar geometry for a memory application, such as the HP/UCLA architecture or such as in a MagRAM chip. The nanoblock would likely consist of an n by n array of wires that connect at the intersections of the wires to n^2 memory elements. Without multiplexing, 2n external wires are needed to connect to these 2n internal wires. If the wires are forced to remain in a plane, the lithographic leads must lie at the periphery of a square ~nw on a side. The maximum memory density is thus: $n^2 / (nw)^2 = 1/w^2$. Note that this density is determined by the *linewidth w of the lithographic* connections, and not the nanoblock. For 100 nm linewidths, the density is 10 Gb/cm^2. Effectively exploiting higher density crossbar nanoblocks using this simple 2D fanout approach is thus not possible. It is also important to note that there are relatively good technologies for making volatile and nonvolatile memory elements with a size that is only a few linewidths across (capacitors or floating gate devices) and other technologies that are far along in development (MagRAM). Stated simply, there is little to gain in this architecture by making small devices unless one solves the fanout problem.



Configuring the Machine

- Need properties of the elements before can design architecture
  - CMOS very different in fan in/fan out vs bipolar
- If use conventional fan-in/fan-out, machine is basically all interconnects
- Possible solution: configure multi-component nano-element as a processor with both arithmetic function and memory. Address element serial through small number of lines

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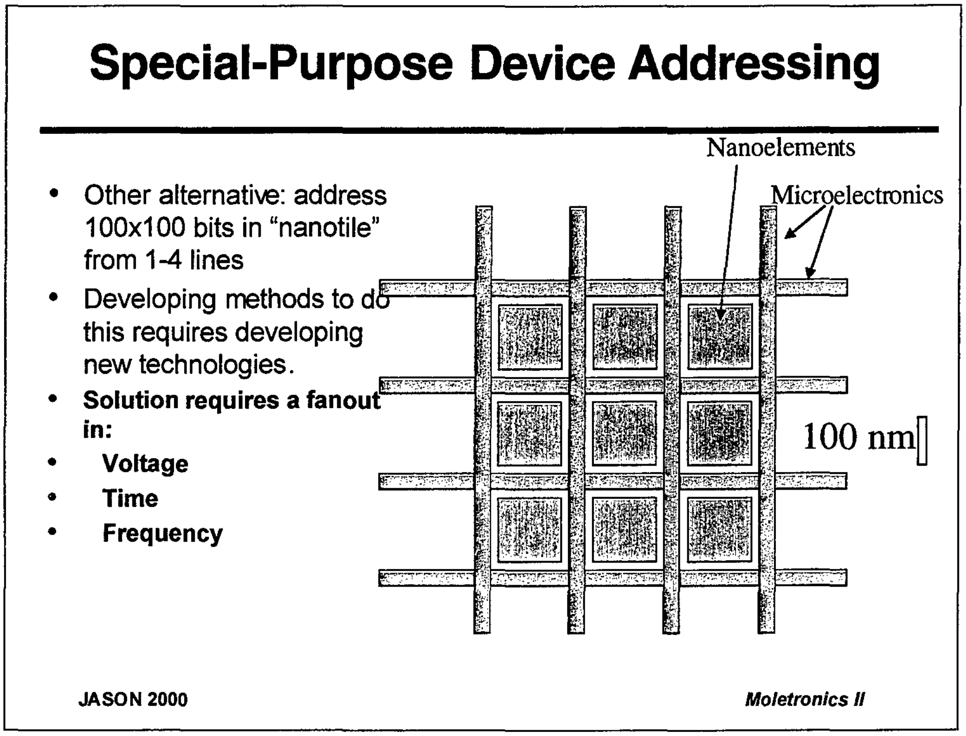
II.B.1.c Fan out

If we allow the nanoblock or the lithographic wires to leave the plane, the situation appears more favorable. For example, the 2n wire pads can be packed as a 2-D grid into a square $w(2n)^{1/2}$ on a side. The nanobloc will connect to these pads in the third dimension. The density is then: $n^2/(2nw^2) = (n/2)(1/w^2)$. This geometry thus provides a linear (in the number of wires in the nanobloc) gain in density over what can be done with straight lithography in 2D. (How to connect the nanoblock to the pads is of course an unsolved practical problem.)

However this limiting gain is likely an overstatement. Each nanoblock wire requires electronics to read it – a CMOS amplifier at least - and probably something better. The linear footprint of these amplifiers will be many units of the basic linewidth of the CMOS process. This footprint may (in fact, probably will) dominate over the area devoted to the crosspoint array. Once again, little is gained by miniaturizing the crosspoint array all by itself. One either has to miniaturize the amplifiers, interconnects, etc. as well, or multiplex one lithographic lead to many nanowires. Multiplexing is a natural response to fan-out problems, but it compounds the issues of line-leveling amplifiers.



Special-Purpose Device Addressing

- Other alternative: address 100x100 bits in "nanotile" from 1-4 lines
- Developing methods to do this requires developing new technologies.
- **Solution requires a fanout in:**
- **Voltage**
- **Time**
- **Frequency**

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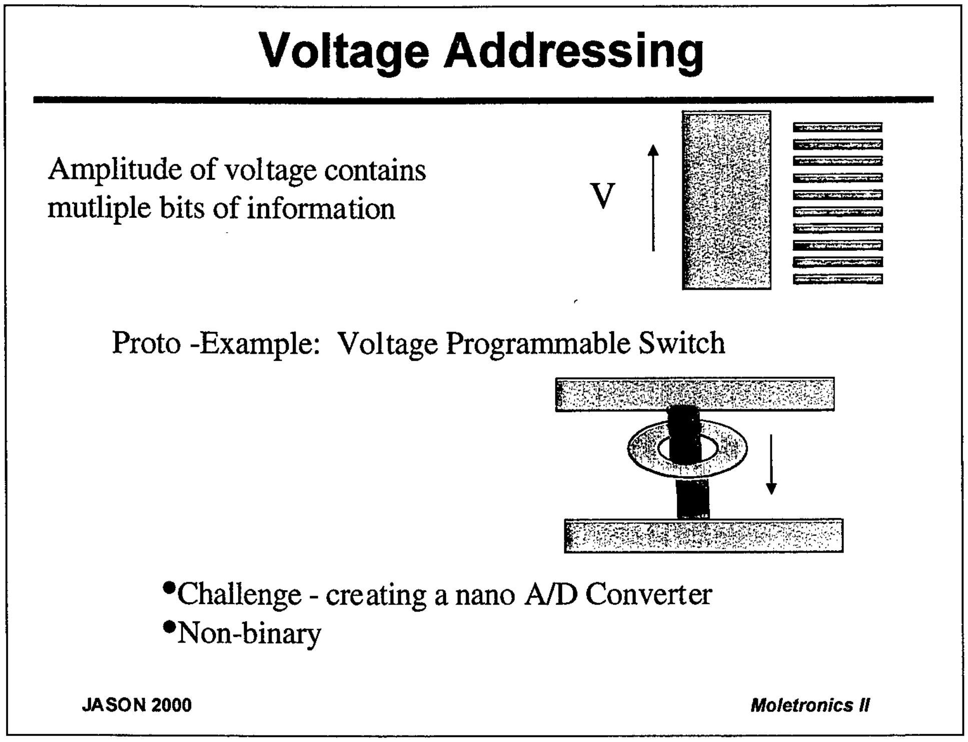
II.B.1.d Multi-state device addressing

As discussed in the preceding section, addressing multiple lines in a nanoblock with one lithographic lead ("multiplexing") offers a potential solution to the I/O problems discussed in Section II.B.2c. To accomplish this multiplexing, a number of approaches can be imagined. This is a critical area for future study. Such multiplexing is of general interest in nanotechnology, where a few macroscopic elements are trying to read/control a larger number of molecular components. A few possible conceptual approaches are schematically illustrated in the following.



Voltage Addressing

Amplitude of voltage contains
mutliple bits of information

Proto -Example: Voltage Programmable Switch

- Challenge - creating a nano A/D Converter
- Non-binary

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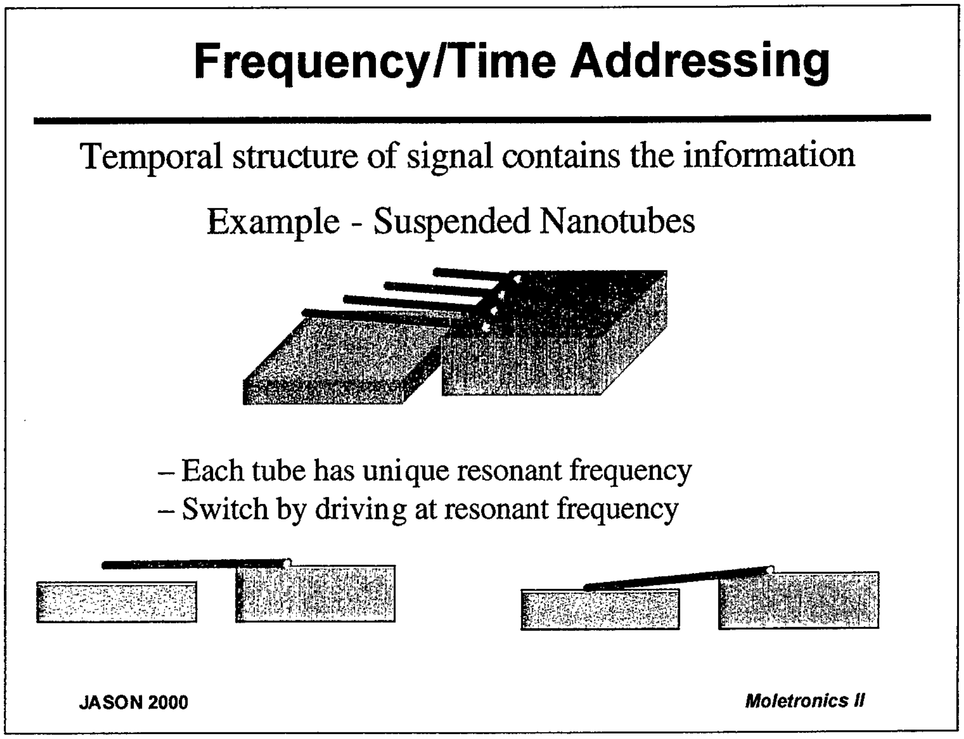
II.B.1.d Multi-state device addressing

Voltage Addressing – the amplitude of the voltage signal could contain multiple bits of information. In essence, the nanoblock must effectively serve as an A/D and D/A converter, in addition to its other functions. The challenge is constructing a device/architecture that can effectively perform this function. A simple example is using a large voltage on a line to write a bit while using a small voltage on the same line to read it. Moving beyond this simple version is another interesting problem for future study.

One such example might be envisioned by perturbing the basic structure of the HP/UCLA approach, and preparing a series of molecules such that the members of the series only switched conductance states above some ever increasing set of voltage thresholds. Of course, isolating these thresholds from one another would require significant separation in voltage, so that writing and reading a bit for processing applications would be extremely energy-intensive. We thus reach the same conclusion as before, that such systems seem suited at best to high density memory devices but not for processing/computation. The associated challenge is to obtain a sufficient number of different, isolable levels so that the density gains (relative to the CMOS amplifier line spacing needed to drive the I/O lines to the nanoblock) are large enough to offset the increased cost that will be associated with physically interfacing the nanoblock technology to CMOS technology.



Frequency/Time Addressing

Temporal structure of signal contains the information

Example - Suspended Nanotubes

- Each tube has unique resonant frequency
- Switch by driving at resonant frequency

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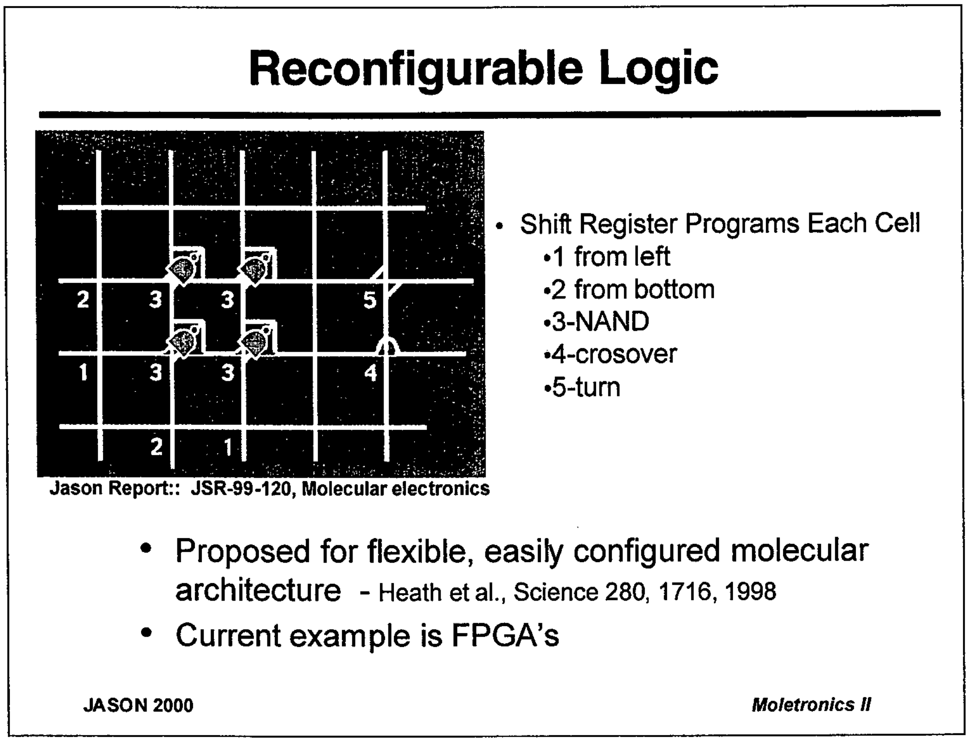
II.B.1.d Multi-state device addressing

Frequency/Time Addressing – The general approach here is to use the temporal structure of a voltage signal to address a particular element. This approach certainly has precedent in both radio and optical communications systems, where different frequencies carry different bits of information. The massive parallelism that this gives in a fiber optic cable is legendary. A key challenge here is creating a nano-resonator that selects for a particular frequency.

In the example shown in the Figure, a vibrating nanotube might serve as the resonant element in a frequency-selective switch. Tubes with different lengths would vibrate at different frequencies. For a 100 nm long single-walled nanotube (SWNT), the resonant frequency, f_0 is expected to be ~ 1 GHz. Driving the tube electrostatically at its resonant frequency would cause the tube to oscillate and switch between two metastable states. The Q of the oscillator determines the bandwidth $\delta f = f_0/Q$ required for each tube and hence the overall amount of multiplexing possible. δf also determines the characteristic switching frequency. For a Q ~ 100 (consistent with experimental measurements on nanotubes), the switching frequency is 10 MHz. Clearly, it would be desirable to construct even higher frequency oscillators to lower the switching times and increase the overall available bandwidth. Again, much lower clock rates are attainable in practice due to the need to address many tubes from one I/O wire.



Reconfigurable Logic

- Shift Register Programs Each Cell
  - •1 from left
  - •2 from bottom
  - •3-NAND
  - •4-crosover
  - •5-turn

Jason Report:: JSR-99-120, Molecular electronics

- Proposed for flexible, easily configured molecular architecture - Heath et al., Science 280, 1716, 1998
- Current example is FPGA's

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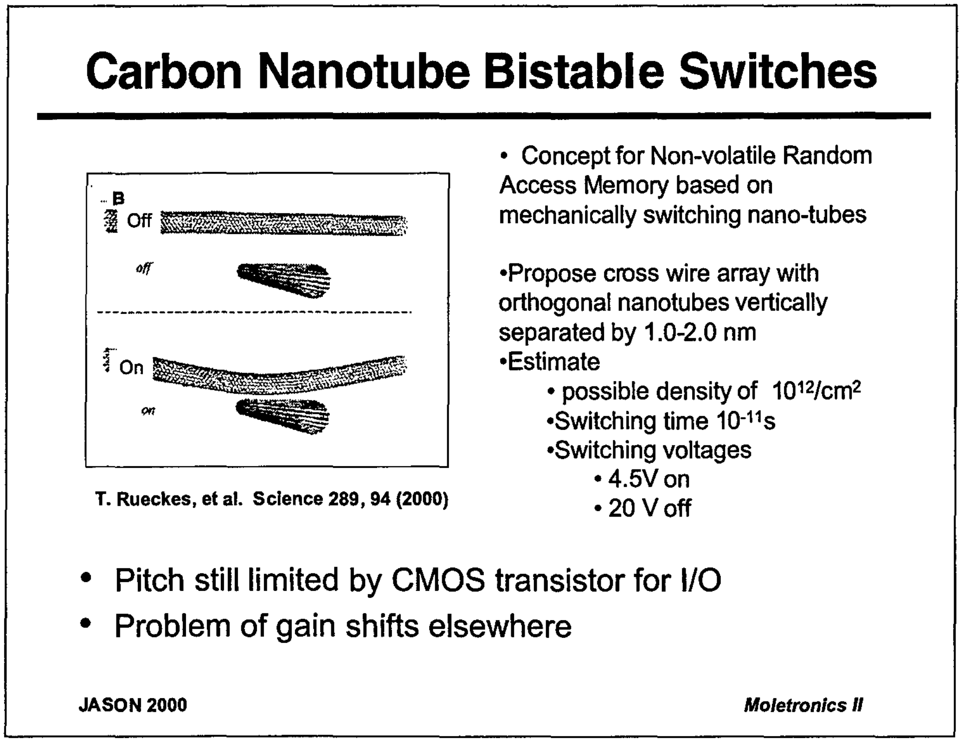
II.B.2 Architecture

II.B.2.a Defects/Configurable logic

We now turn to issues related to architectures that have been proposed for high density molecular electronic devices. One proposed approach to dealing with defective structures is to model molecular electronic devices around FPGA's. In this approach, a general purpose machine is a series of look-up tables, and the hardware is configured by application of electric fields to certain positions in the array. A shift register can program each cell; provided that a diode is present at each interconnection point, it can be shown that the device can be configured to perform arbitrary logic functions. In this approach, the devices might even be individually programmed to account for the individual defect structures internal to each nanoblock.

The performance issues associated with FPGA's do not lend themselves well to increased density devices for processors construction. According to Rent's rule, increasing the density results in a device that is almost all interconnects. Rent's rule is an empirical rule that has been found to hold for a large collection of chip designs.

The possibility of using FPGA's productively requires good information about the nature and distribution of the defects. At present there have been no studies of defect modes in either the fabrication stage or during operation. Serious evaluation of potential architectures will not be possible until such information is available.



Carbon Nanotube Bistable Switches

T. Rueckes, et al. Science 289, 94 (2000)

- Concept for Non-volatile Random Access Memory based on mechanically switching nano-tubes

- Propose cross wire array with orthogonal nanotubes vertically separated by 1.0-2.0 nm
- Estimate
  - possible density of $10^{12}/\text{cm}^2$
  - Switching time 10^{-11}s
  - Switching voltages
    - 4.5V on
    - 20 V off

- Pitch still limited by CMOS transistor for I/O
- Problem of gain shifts elsewhere

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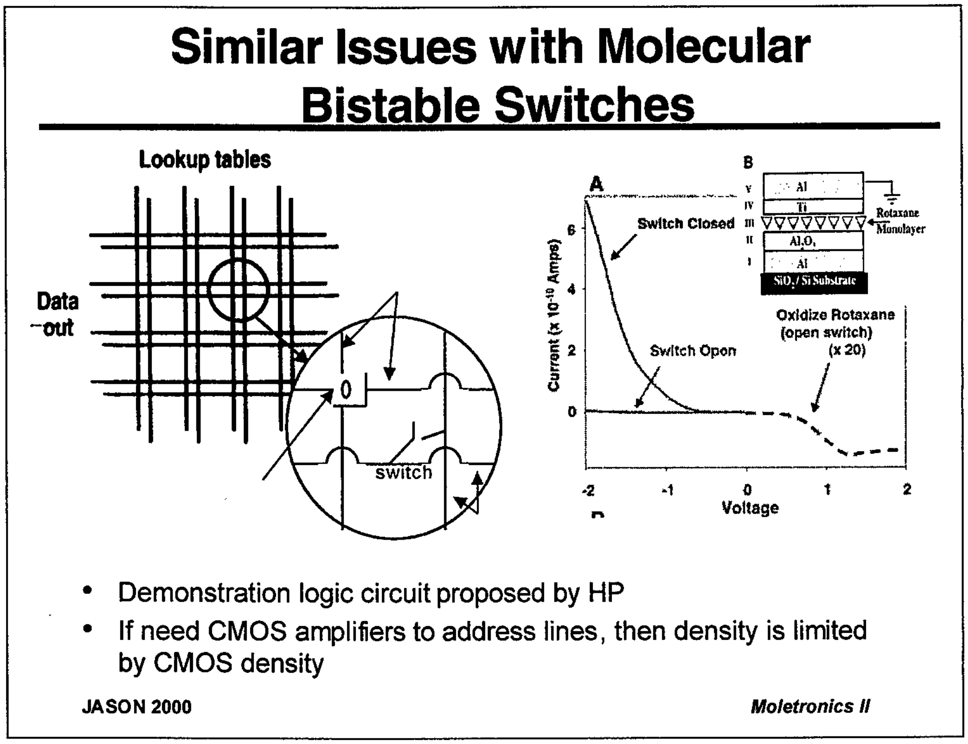
II.B.2. b Proposed demonstration logic circuits

There has been a great deal of progress in creating individual nanoelectronic devices. For example, bistable switches that can be written/read electrically have been proposed and realized using different approaches (see the figure above and the one that follows). Both examples utilize the physical motion of a molecule (rotaxane or nanotube) to change the state of the system. Such devices have been operated in a laboratory setting, and there is room for optimism that they can be made reliably and reproducibly. See: T. Rueckes *et al.*, Science **289**, 94 (2000); C.P. Collier *et al.*, Science **289**, 1172 (2000).

Testing such molecular devices in simple cross-bar architectures provides a sensible venue for evaluating many of the technical issues (e.g. power dissipation, switching rate, line RC, defect rate) that must be resolved for molecular electronics.



Similar Issues with Molecular Bistable Switches

- Demonstration logic circuit proposed by HP
- If need CMOS amplifiers to address lines, then density is limited by CMOS density

II.B.2. b Proposed demonstration logic circuits (cont'd)

Arranging molecular-scale devices in a way that allows for high density storage and/or computing remains an unsolved problem. The nanoblock crosspoint architectures discussed above are passive and lossy. External amplifiers are therefore needed to restore the signal levels of the outputs of the array so that they can drive the inputs of another array. If standard CMOS amplifiers are used for this task, with one amplifier per nanowire, the area required for the amplifiers dominates (see II.B.1.c). In this case there is little or no benefit to using molecular scale arrays.

One solution to this problem would be to incorporate gain into the nanoblock to restore signal levels. Then one nanoblock could drive the next without the need for an intervening level of CMOS. This presents two major technical challenges. The first is to achieve the necessary gain within the nanoblock to drive its outputs. The second is to develop schemes to wire these nanoblocks together without an intervening lithographic level. Both of these are extremely challenging problems.

Electrical Properties of Molecular Systems

- Switching Energy
  - Device Alone and Device + Contacts
- Bit Rate
  - Interconnect RC and Contact RC
  - Device switching rate
- Defect/Failure Rate
- Architecture
  - Serial vs. parallel operation
  - What can be done if gain must be provided at CMOS size scale?
  - What can be done with real molecular devices?

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II.B.2.c Architecture design requires knowledge of device properties

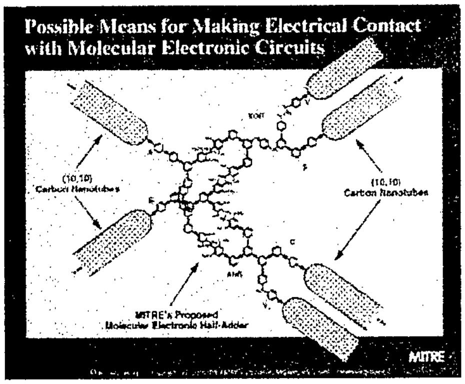
We now turn to an evaluation of the properties of molecular electronic devices that have been explored or proposed to date.

Discussions of architectures and applications for potential molecular electronic circuits have largely been shaped by analogies to silicon-based integrated circuits. This mind set seems to have been shaped by the notion that molecular devices will be equivalent (but smaller) replacements for the electronic devices that we all learned about in undergraduate electronics courses. Specifically, the idea that unconjugated organic molecules are "like" resistors, and that conjugated molecules are "like" conductors seems to have been translated into a notional quantitative identity. In addition, an insulating gap bridged by a molecule has been equated with a rectifying diode or a resonant tunnel diode.

The assumption that molecular devices must act like traditional devices is an impediment to developing practical applications. Fortunately, a wealth of information already exists about electronic transport in molecules from work in analytical and physical chemistry. Thus, it is already quite feasible to formulate descriptions of molecular devices based on a realistic description of their electron transport properties.

What might be done with Suggested Devices?

- Illustrative Electronic Circuit based on Suggested Molecular Devices
  - Circuit contains notional molecular resistors, conductors and resonant tunneling diodes.
  - No gain
  - Size ca. 4 nm x 4 nm
  - Unresolved issues of element isolation, electric field distribution, dissipation
  - Unresolved issues of molecular assembly and contacts to electrodes

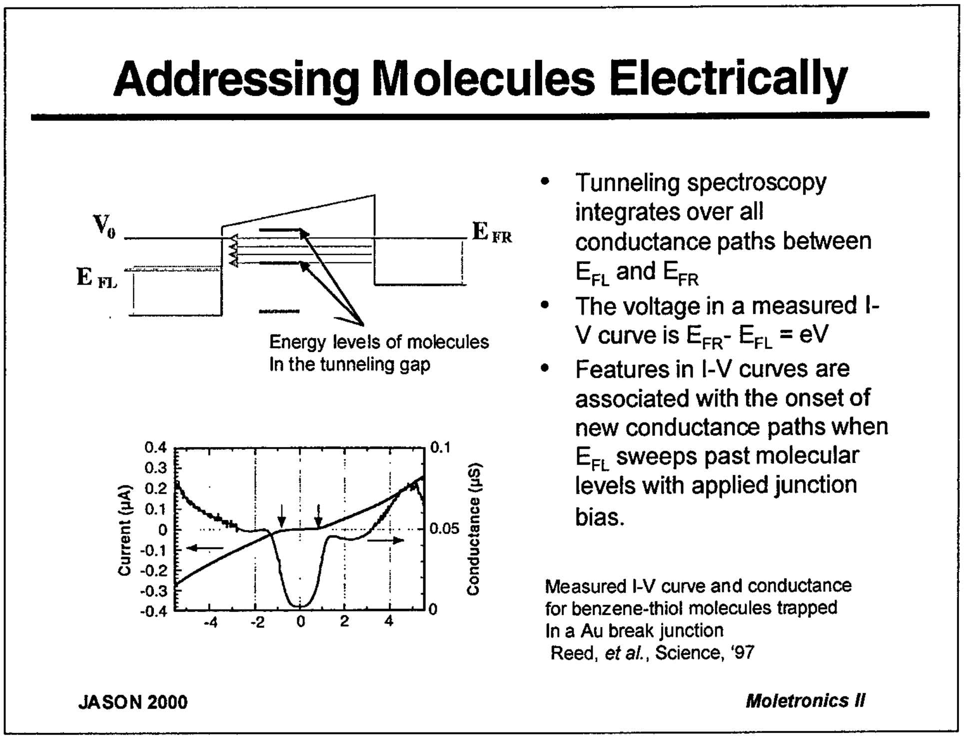


J.C. Ellenbogen, J.C. Love,
Proc. IEEE, March 2000, pp. 386-426

II.B.2.c Architecture design requires knowledge of device properties

The types of molecular devices that would be required to emulate silicon-based devices have been described by Ellenbogen and co-workers. As illustrated above, construction of a half-adder from notional molecular resistors, conductors and rectifying diodes would require a complex organic synthesis, perfect control of the geometry and formation of six electrical contacts to external wiring.

This analysis gives some insight into the size scale and complexity of potential molecular devices that might result if one insists on emulating silicon-based devices. Futhermore, as discussed in the following sections, enough is already known about molecular electron transport to understand that molecules will not respond like simple devices. Thus, the design of any functional molecular circuitry will require adapting to the available properties of molecules.



Addressing Molecules Electrically

Energy levels of molecules
In the tunneling gap

- Tunneling spectroscopy integrates over all conductance paths between E_{FL} and E_{FR}
- The voltage in a measured I-V curve is $E_{FR} - E_{FL} = eV$
- Features in I-V curves are associated with the onset of new conductance paths when E_{FL} sweeps past molecular levels with applied junction bias.

Measured I-V curve and conductance
for benzene-thiol molecules trapped
In a Au break junction
Reed, *et al.*, Science, '97

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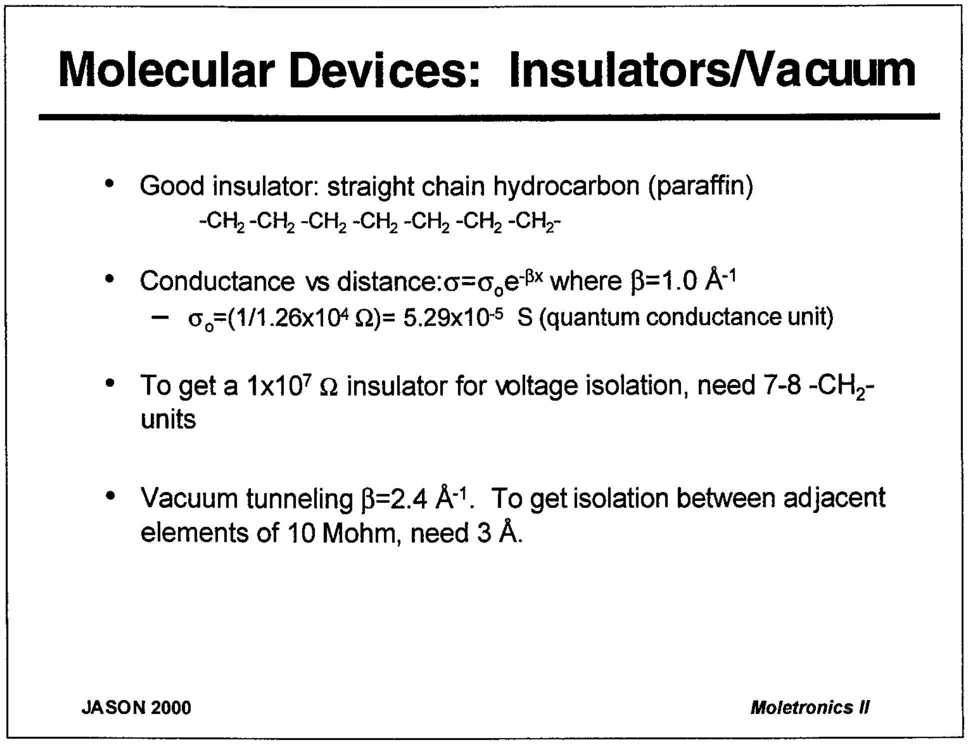
II.B.3 Molecular Device Properties

Studies of electron transport through molecules have a long history in several scientific disciplines. As a result there is a significant body of information already available that would be useful in understanding fruitful directions of the development of molecular electronics.

II.B.3.a Addressing molecules electrically

To transport electrons through a molecule requires making electrical contacts at the two ends of the molecule, in a configuration illustrated schematically in the top panel above. The molecular energy levels (properly aligned by aligning the molecular vacuum level and the vacuum levels of the two electrodes) then appear in the gap. Application of an electrical bias across the gap shifts the Fermi levels of the electrodes, allowing electron tunneling from the filled density of states of one electrode into the empty density of states of the opposite electrode. If an energy level of the molecule is located in the energy range between the Fermi levels of the two electrodes, then enhanced tunneling can occur via resonance with the state. Because the total current is an integral over all of the accessible density of states, as the bias voltage sweeps past such resonant molecular levels, the effect on the measured current does NOT appear as a discrete feature in the measured I-V response. Thus, negative differential resistance is not commonly the result of resonant tunneling in a metal-insulator-metal junction. Instead smooth I-V curves, as measured for benzene-thiol molecules bonded between gold electrodes, are expected. (For a long molecule, some molecular energy levels may be localized at different lateral positions in the gap, which would cause a differential response of the different energy states to fields applied across the gap, and thus the possibility of resonant features displaying negative differential resistance.)



Molecular Devices: Insulators/Vacuum

- Good insulator: straight chain hydrocarbon (paraffin)
  $-CH_2-CH_2-CH_2-CH_2-CH_2-CH_2-CH_2-$
- Conductance vs distance: $\sigma=\sigma_0 e^{-\beta x}$ where $\beta=1.0$ $Å^{-1}$
  - $\sigma_0=(1/1.26\times10^4\ \Omega)= 5.29\times10^{-5}$ S (quantum conductance unit)
- To get a $1\times10^7\ \Omega$ insulator for voltage isolation, need 7-8 $-CH_2-$ units
- Vacuum tunneling $\beta=2.4$ $Å^{-1}$. To get isolation between adjacent elements of 10 Mohm, need 3 Å.

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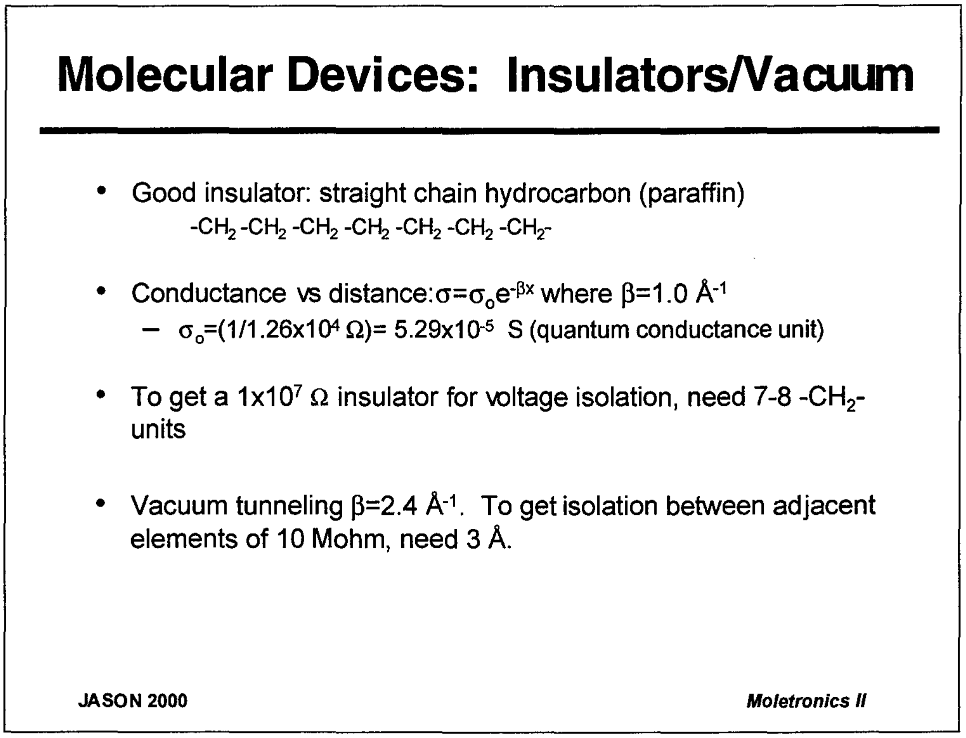
II.B.3.b Real insulator/resistor properties

The electron tunneling/transmission properties of molecules are reasonably well-understood from measurements on intramolecular organic, inorganic, and biological systems that contain electron donors and acceptors located at fixed, known positions and separated by known distances and intervening media. Data are also available for electron transport from a metal electrode to a molecular electron acceptor at a fixed distance from this metal electrode, and for conductance values of STM tips through molecules adsorbed onto metal surfaces. These properties can serve as a guide to the device properties to be expected for molecular electronic systems.

Some of the best organic insulators are straight chain hydrocarbons (paraffins). Electron transmission through the tunnel barriers formed by such molecular linkages, as determined by investigating electron transfer processes in molecular electron donors and molecular electron acceptor systems that are separated by variable-length hydrocarbon spacers, typically falls off with an attenuation factor, β, of ~1.0 $Å^{-1}$. The maximum value of the conductance is obtained from the quantum of resistance, so the dependence of the conductance of such an insulating element on distance is:

$$\sigma = \sigma_0 \exp(-\beta x).$$

To obtain a prototypical 10 M-ohm insulator for voltage isolation between elements in a logic circuit, this indicates that one would require 7-8 carbon units in chain length.



Molecular Devices: Insulators/Vacuum

- Good insulator: straight chain hydrocarbon (paraffin)
  $-CH_2-CH_2-CH_2-CH_2-CH_2-CH_2-CH_2-$
- Conductance vs distance: $\sigma=\sigma_o e^{-\beta x}$ where $\beta=1.0$ Å^{-1}
  - $\sigma_o=(1/1.26\text{x}10^4\ \Omega)= 5.29\text{x}10^{-5}$ S (quantum conductance unit)
- To get a $1\text{x}10^7\ \Omega$ insulator for voltage isolation, need 7-8 $-CH_2-$ units
- Vacuum tunneling $\beta=2.4$ Å^{-1}. To get isolation between adjacent elements of 10 Mohm, need 3 Å.

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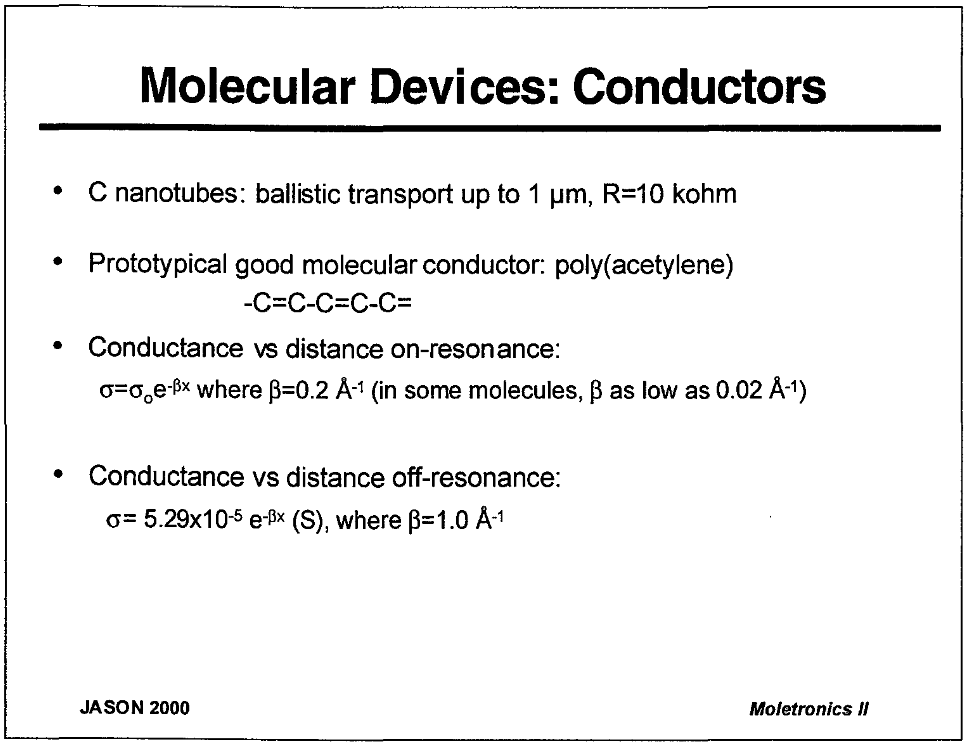
II.B.3 Molecular Device Properties

For comparison, for vacuum tunneling, the attenuation factor is ~2.4 Å^{-1}. So to produce a voltage isolation of 10 M-ohm between adjacent units, one needs a spacer distance of 3 Å in vacuum (larger in water or hydrocarbons) between molecular device elements.

These distances affect not only the size of the molecular electronic devices but also the separation between the contact leads. The increased separation needed for large resistance in the off-state will increase the potential that must be applied to achieve any resonant tunneling through a molecular RTD-type device that is hooked up in series with a resistive element.



Molecular Devices: Conductors

- C nanotubes: ballistic transport up to 1 μm, R=10 kohm
- Prototypical good molecular conductor: poly(acetylene)
  -C=C-C=C-C=
- Conductance vs distance on-resonance:
  $\sigma=\sigma_0 e^{-\beta x}$ where $\beta=0.2$ Å^{-1} (in some molecules, β as low as 0.02 Å^{-1})
- Conductance vs distance off-resonance:
  $\sigma= 5.29\times10^{-5}\, e^{-\beta x}$ (S), where $\beta=1.0$ Å^{-1}

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II.B.3.c Real conductors

We now turn to the properties of organic conductors: so-called "molecular wires". For carbon nanotubes, the transport has been shown to be ballistic for distances up to 1 micron, with resistances of ~12 kohm. A prototypical good molecular organic conductor, exemplified by polyacetylene, has a conductance vs distance characteristic (at energies on resonance with its lowest unoccupied molecular orbital levels) that is given by:

$$\sigma = \sigma_0 \exp(-\beta x)$$

with $\beta=0.2$ Å^{-1}.

Such a molecule of course also has an off-resonance tunneling contribution in addition, which is characterized by $\beta\sim1.0$ Å^{-1}.

Molecular Devices

- Tunnel Diodes

  Driving into/out of resonance depends on electric potential drop across molecule

    Requires large fields, I.e. higher voltages as molecules get larger

  Electronic level bandwidths in molecules are typically >0.5 eV

  Thus, requires >>0.5 eV to switch from non-resonant state to resonant state and back again in RTD

- Summary of Molecular Devices

  Compared to Si, molecular elements will be more dissipative, less rectifying, require higher switching voltages, and lack gain

II.B.3.d Real diodes

The observation of apparent (see Sections II.B.5 or 6) resonant features in the I-V characteristics of tunnel junctions containing molecules have suggested applications of such systems as resonant tunnel diodes.

The values in the charts above are useful because they illustrate both the dissipation as well as the limitations on RC time constants that would be imposed through the use of molecular wires, as opposed to the bulk metallic Cu wires that are employed in present VLSI devices. These values also allow computation of the electric potential that is required to be applied in order to a) reach resonant tunneling properties with the conductive elements of the system; b) drive any RTD molecular elements into resonance and the dissipation that will be associated with the use of such high potential differences through such molecular wire resistive elements, and c) the associated switching times of such systems. Another factor that also needs to be considered is the electronic coupling between the pi orbitals of the "wires" and the sigma orbitals of the "insulators" because this coupling can be a significant tunnel barrier as well (i.e., contacts between molecular wires and molecular diodes are not well characterized to date). These calculations can not be done in general but can (and recently have been) done for specific systems to evaluate electrical behavior, such as the I-V characteristic.

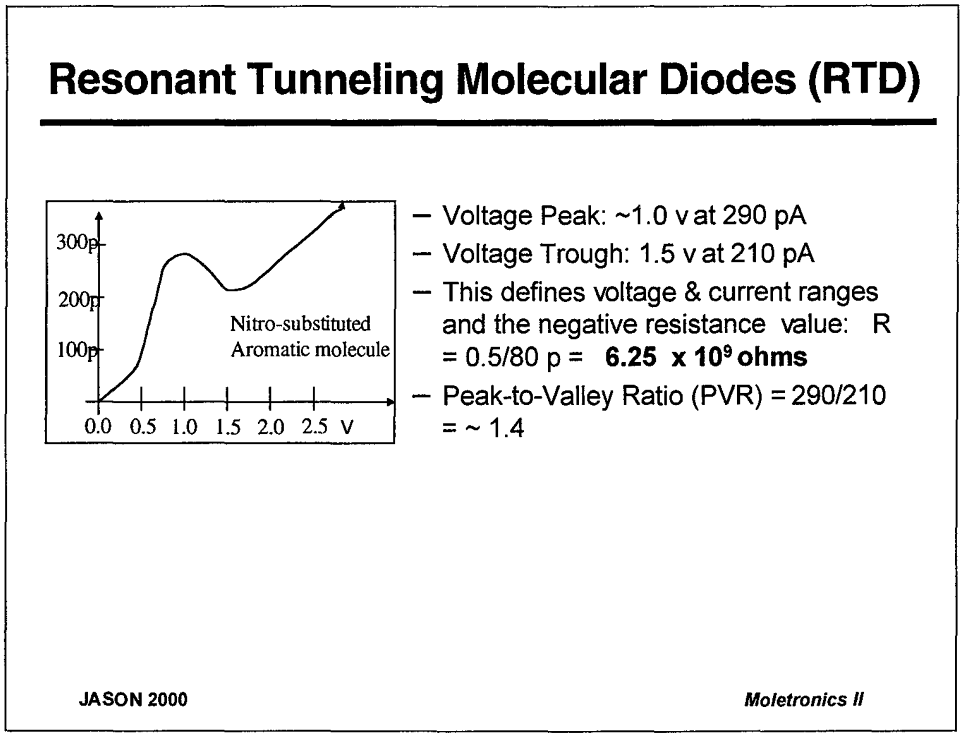
Need for Performance Diagnostics

- An electrical engineering evaluation of molecular device properties is critical to development of viable architectures
- Don't require/assume
  "Just the same as Si only Smaller"
- Reproducibility and lifetime of molecular device properties must be evaluated
- Contact issues are critical

II.B.4 Performance Diagnostics

The synopsis in the previous section clearly shows that molecular electronic properties are not simply scaled down versions of standard electronic components. If a molecular architecture is to be developed, it will have to be based on actual molecular properties.

To advance the field, therefore, a careful charactrization of molecular device properties from an electrical engineering standpoint should be a standard procedure in molecular electronics research. As an illustration of such an analysis, we present an analysis of a recently reported molecular RTD.



Resonant Tunneling Molecular Diodes (RTD)

- Voltage Peak: ~1.0 v at 290 pA
- Voltage Trough: 1.5 v at 210 pA
- This defines voltage & current ranges and the negative resistance value: R = 0.5/80 p = **6.25 x 10^9 ohms**
- Peak-to-Valley Ratio (PVR) = 290/210 = ~ 1.4

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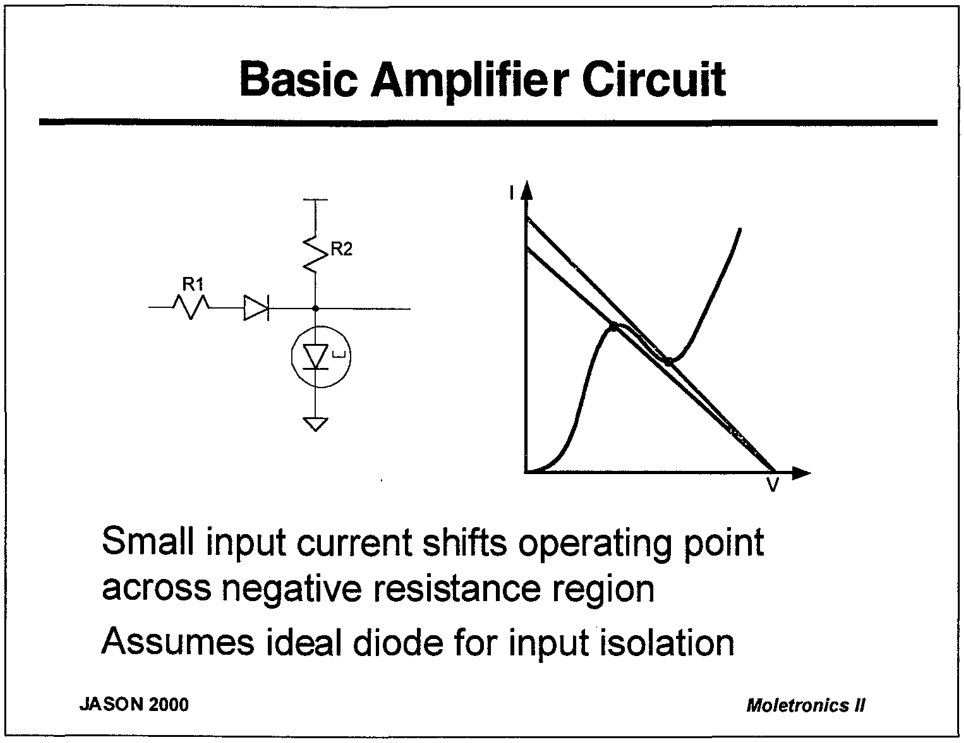
II.B.4 Performance Diagnostics

Apparent resonant features, e.g. local maxima displaying a region of negative differential resistance (NDR) have been observed in a few molecular tunneling current-voltage (I-V) measurements, leading to the suggestion that molecular electronic resonant tunnel diodes can be fabricated. Analysis of the device properties based on the measured behavior of such junctions is however required to evaluate the feasibility of any possible applications. As an illustration of such an analysis, we here consider the reported characteristics of a junction displaying a NDR feature at room temperature, and what types of circuits would be required to exploit its assumed RTD behavior.



Basic Amplifier Circuit

Small input current shifts operating point across negative resistance region

Assumes ideal diode for input isolation

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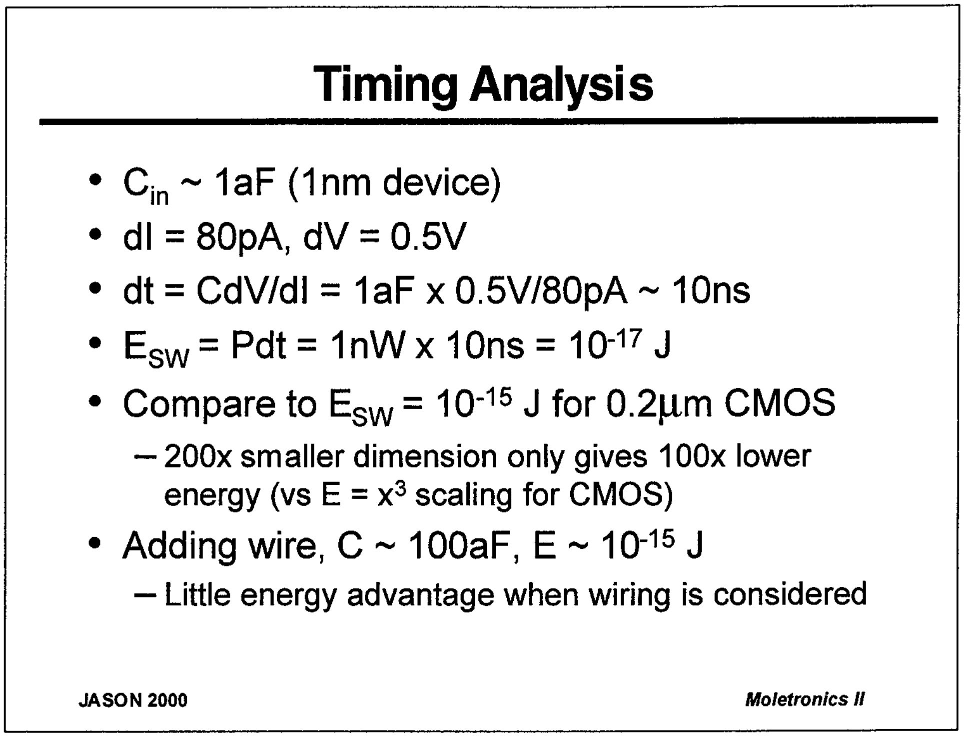
II.B.4 Circuit Analysis of Molecular Device Properties

Since the lack of any gain-producing capability in molecular systems is one of the crucial issues in molecular electronics, we consider the possibility of using the molecular "RTD" as a gain producing element. A configuration which can accomplish this is illustrated above. The RTD is configured with a bias voltage dropped across a load resistor R2 at its input. The bias voltage and load resistance must be chosen to place the RTD in the NDR region of its I-V curve.

At this point, the application of a voltage across the input resistor R1 creates an increased current and thus a decreased voltage across the diode. The voltage response is thus basically a voltage modulation proportional in magnitude to the input voltage sumperimposed on the operating voltage of the RTD. Appropriate choice of the balancing resistors R1 and R2 allow the input voltage to be amplified within the limited voltage range of the diode NDR.



Timing Analysis

- C_{in} ~ 1aF (1nm device)
- dI = 80pA, dV = 0.5V
- dt = CdV/dI = 1aF x 0.5V/80pA ~ 10ns
- E_{SW} = Pdt = 1nW x 10ns = 10^{-17} J
- Compare to E_{SW} = 10^{-15} J for 0.2μm CMOS
  - 200x smaller dimension only gives 100x lower energy (vs E = x^3 scaling for CMOS)
- Adding wire, C ~ 100aF, E ~ 10^{-15} J
  - Little energy advantage when wiring is considered

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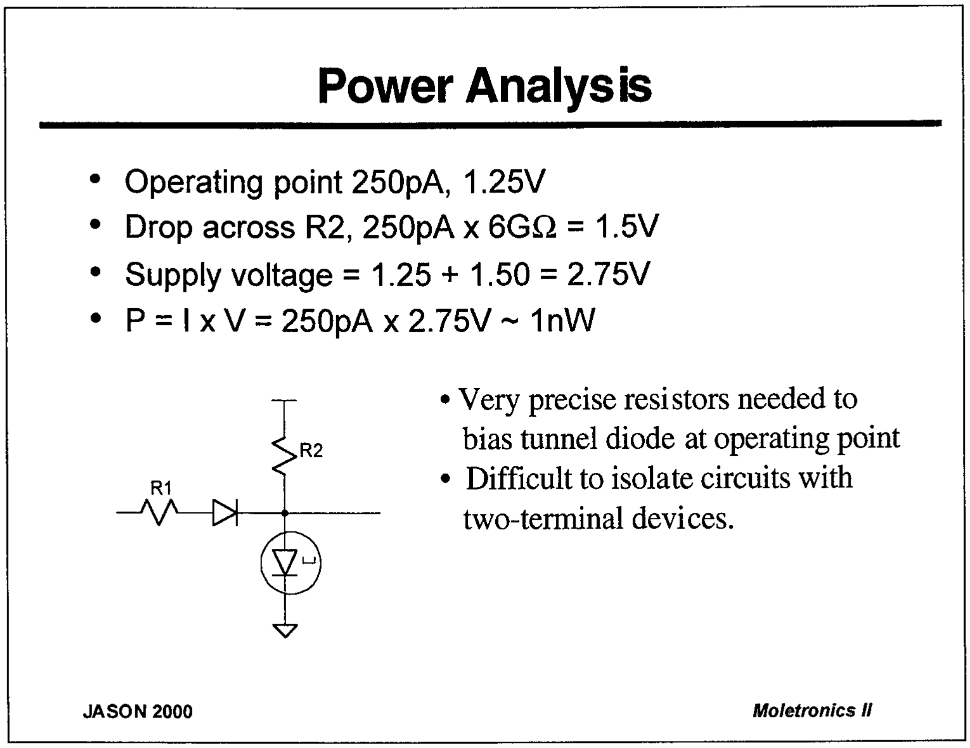
II.B.4 Performance Diagnostics

The operating characteristics of the RTD amplifier are set by the input capacitance and by the current-voltage characteristics of the NDR region. As shown above, under ideal operating conditions, the switching energy could be as low as ~$2x10^3$ kT. However, the need to drive the capacitance of the output wire increases the switching energy to a value comparable to that of state-of-the art CMOS, ~$2x10^5$ kT.



Power Analysis

- Operating point 250pA, 1.25V
- Drop across R2, 250pA x 6GΩ = 1.5V
- Supply voltage = 1.25 + 1.50 = 2.75V
- P = I x V = 250pA x 2.75V ~ 1nW

- Very precise resistors needed to bias tunnel diode at operating point
- Difficult to isolate circuits with two-terminal devices.

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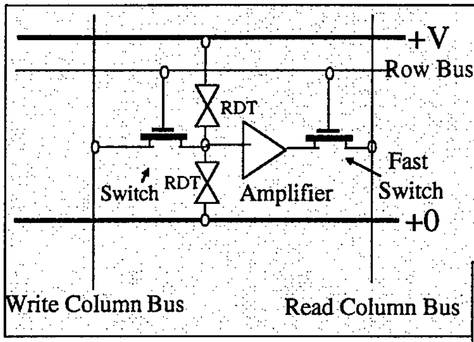
II.B.4 Performance Diagnostics

In addition to the switching energy, one must consider the steady power draw due to the bias voltage across the load resistor and the diode. To obtain gain, the value of the load resistor should be comparable to the dynamic resistance of the RTD, in this case about 6 Gohm. The value of R2 then determines the value of the bias voltage, in this case about 2.75 V, needed to maintain the RTD in its operating range. The result is a steady state power of about 1 nW per device.

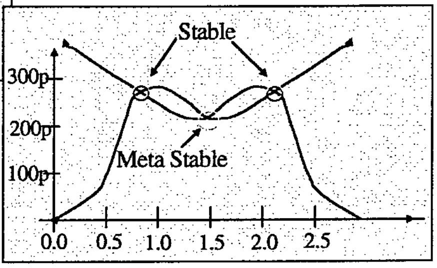
A related issue is that molecular spectroscopy clearly indicates that the line widths are on the order of 0.5 eV for electronic states of organic molecules at room temperature. Thus, molecular electronic RTD devices made from such materials will necessarily need to be run at >1 V to be biased initially at their maximum conductance values, and will require at least 0.5 eV of switching energy to reach the low conductance value where these broad states are placed out of resonance. Additionally because the contribution to the conductance from the nonresonant states is much higher than that in VLSI-based devices (due to the small separation between contacts of molecular devices facilitating leakage currents through tunneling), the on-off ratio of such RTD's is expected to be low.

Implementation of such an amplifier is highly sensitive to the values of the resistors R1 and R2, and to placement in the surrounding circuitry which might cause perturbing current loads. Also, a power drian of 1 nW per device sets an upper bound of ~ 10^{11} devices/cm^2 to maintain heat dissipation at a level of < 10^2 W/cm^2.

Memory Cell Using RTD



Based on measured molecular
RTD properties:
A pair in a series connection
across a 2.5V supply
will provide a
flip-flop (memory cell):
'0' = 0.75 v;
'1' = 1.75 v

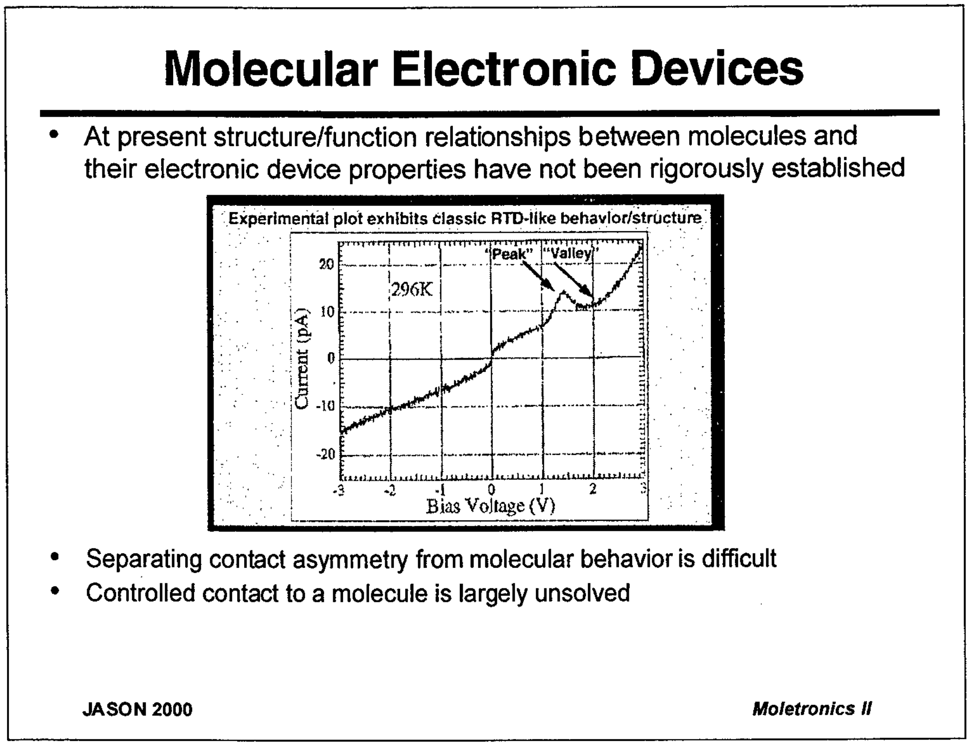


Analogous to SRAM Gain cell
Fabricated with InP-based RTD
Operates at ~ 100 nA, 0.45V
Van der Wagt, Seabaugh, Beam
Texas Instruments

II.B.4 Performance Diagnostics

Semiconductor-based resonant tunnel diodes do have niche applications, and numerous proposals have been made for applications in which they can provide superior performance. For instance, research efforts at Texas Instruments have resulted in a device in which a III-V RTD, in combination with transistors and an amplifier, was configured as a flip-flop in a low-stand-by power static RAM.

Molecular electronic RTDs could in principle be utilized in such circuit designs, provided that the molecular properties offered some improved performance/price characteristic for the application of interest.



Molecular Electronic Devices

- At present structure/function relationships between molecules and their electronic device properties have not been rigorously established

Experimental plot exhibits classic RTD-like behavior/structure

- Separating contact asymmetry from molecular behavior is difficult
- Controlled contact to a molecule is largely unsolved

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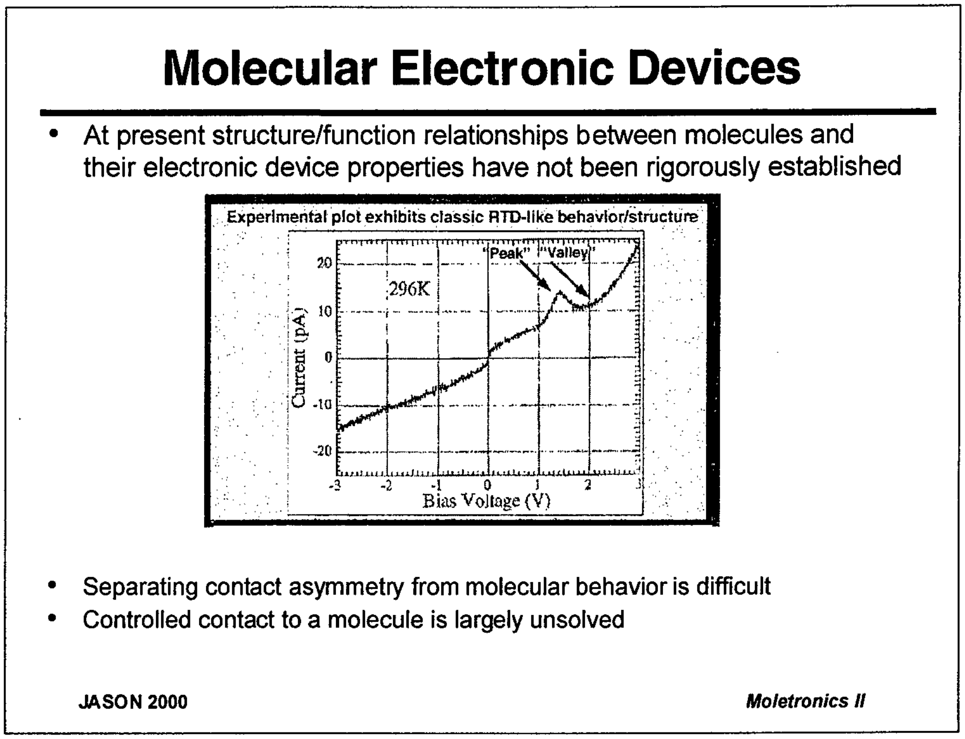
Moletronics II

II.B.5 Understanding Molecular Conductance

Experimental characterization of electronic transport through molecules is generally confounded by issues associated with the nature and reproducibility of the contacts to the electrodes. The most controllable contacts may occur via chemical bonding of a molecule to both electrodes, as is the case for the benzene-thiol molecule illustrated in section II.B.3 and later in this section. Related measurements have been made on SAMs (self-assembled monolayers) in which the molecules are chemically bonded to one surface. The contact to the second electrode is then made either by evaporation of a metal film, or by use of a scanned probe tip.



Molecular Electronic Devices

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Experimental plot exhibits classic RTD-like behavior/structure

- Separating contact asymmetry from molecular behavior is difficult
- Controlled contact to a molecule is largely unsolved

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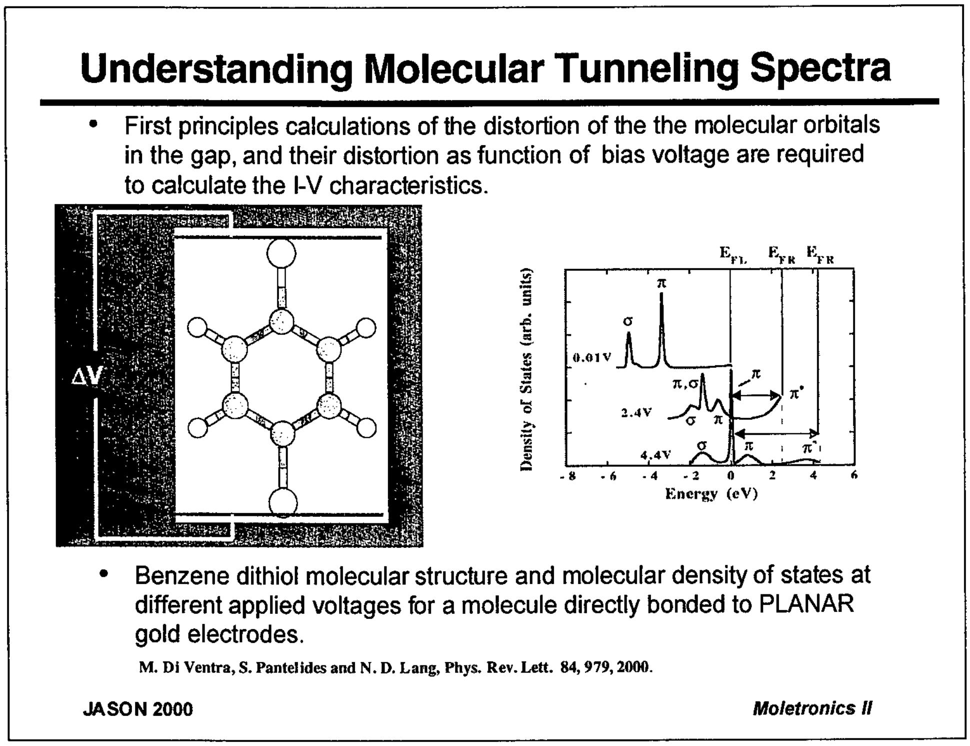
II.B.5 Understanding Molecular Conductance - (cont'd)

Trapped charge states are a well-known problem in silicon dielectrics, where they create temporal noise in the insulating layer. Such trapped charge states have long since been shown (Koch and Hamers, in Physics and Chemistry of SiO_2 and the Si-SiO_2 interface, Eds. C.R. Helm and B. Deal, 1990) to correlate with NDR features in STM I-V spectra measured through thin oxide layers on silicon. The mechanism for the NDR is an increase in tunneling probability as the Fermi level of the source electrode sweeps past the energy level of the trapped charge state.

Once the state is filled, the negative charge in the tunnel junction reduces transmission, causing a temporary decrease in the current and thus the observed negative slope of the I-V curve. In such a situation, the charge-discharge rates of the traps themselves must be considered in evaluating performance of the device. A similar mechanism (voltage-controlled formation of anions of the molecule in the junction) has been proposed as a mechanism to produce strong NDR in molecular electronics (Chen, et al, Science 286 1550 (1999)). The strong temperature dependence of the I-V spectra in this case might suggest that discharge of the trapped electrons becomes rapid at room temperature.

Molecular electronic devices showing NDR features due to such charge trapping/transfer will not be suitable candidates for RTD applications.



Understanding Molecular Tunneling Spectra

- First principles calculations of the distortion of the the molecular orbitals in the gap, and their distortion as function of bias voltage are required to calculate the I-V characteristics.

- Benzene dithiol molecular structure and molecular density of states at different applied voltages for a molecule directly bonded to PLANAR gold electrodes.

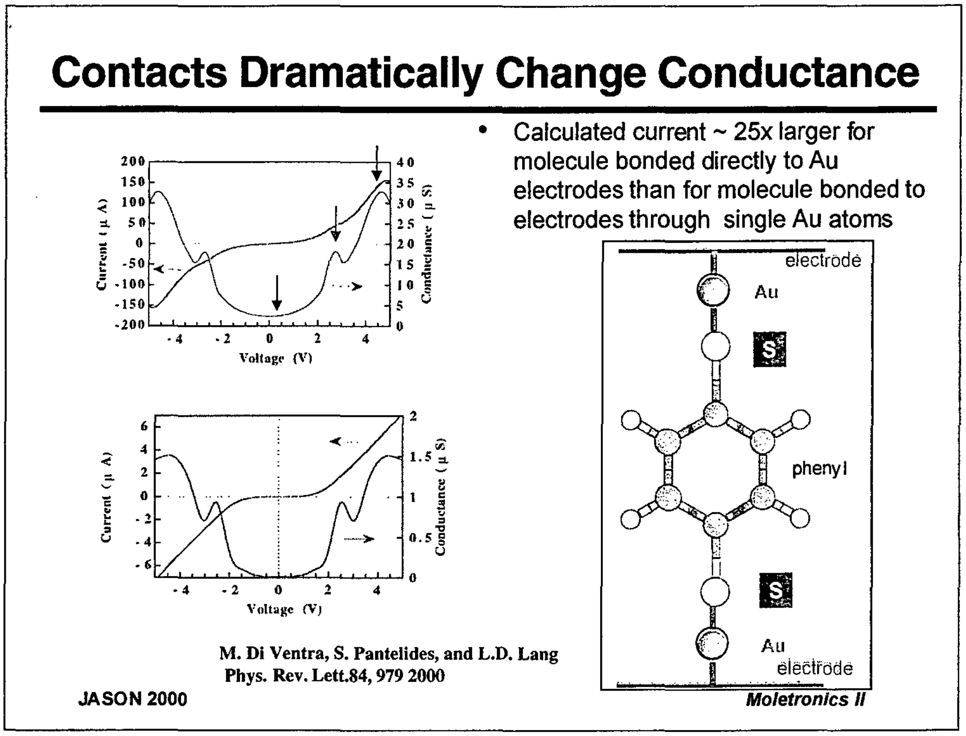
M. Di Ventra, S. Pantelides and N. D. Lang, Phys. Rev. Lett. 84, 979, 2000.

II.B.5 Understanding Molecular Conductance

A zeroth order understanding of tunneling (without charge trapping) through a molecule in a junction can be obtained by assuming 1) that the molecular energy levels are shifted without distortion by the field applied across the junction; and 2) that the molecule is bonded without perturbation to flat "jellium" electrodes. However, recent theoretical work has shown that the real behavior of molecular conductors is much richer and more interesting than predictions based on such simplifying assumptions.

Di Ventra, Pantelides and Lang (DPL) used ab initio methods to calculate the molecular energy levels of a benzene-thiol molecule (as per the experimental work of Reed et al., Science 278, 252, 1997) between gold electrodes. The calculated densities of states, as shown to the right above, change substantially as a potential is applied between the two electrodes. Notably, because different parts of the molecule are at different potentials, the electronic levels due to the sigma and pi orbitals split and overlap.

M. Di Ventra, S. T. Pantelides, N. D. Lang, Phys. Rev. Lett. 84 979 (2000).



Contacts Dramatically Change Conductance

- Calculated current ~ 25x larger for molecule bonded directly to Au electrodes than for molecule bonded to electrodes through single Au atoms

M. Di Ventra, S. Pantelides, and L.D. Lang
Phys. Rev. Lett.84, 979 2000

JASON 2000

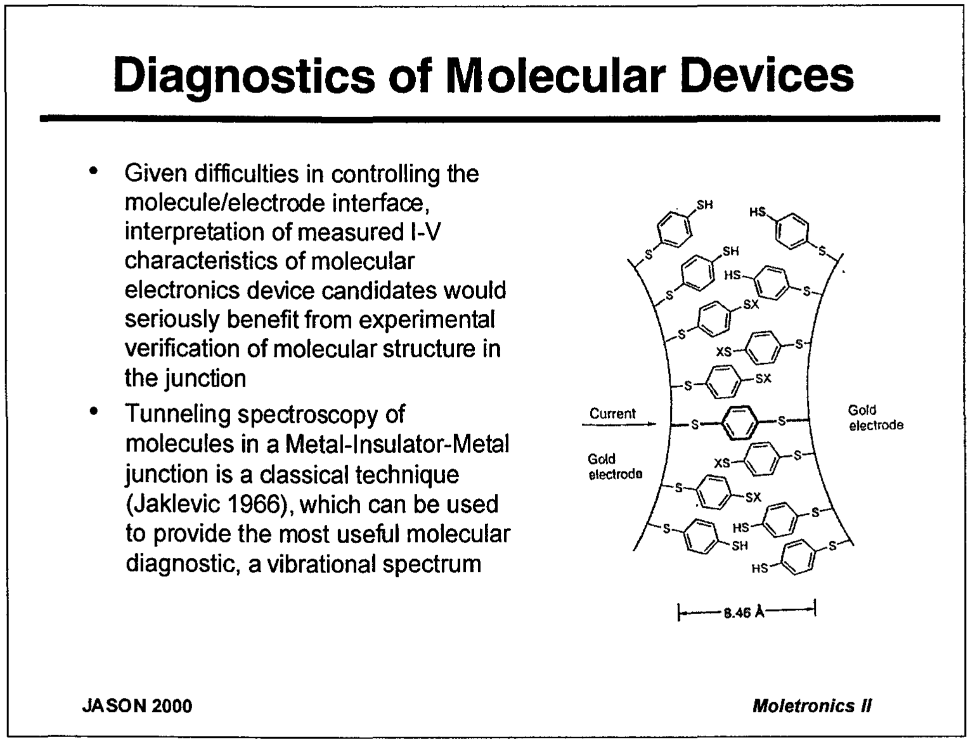
Moletronics II

II.B.5 Understanding Molecular Conductance

The calculated electron densities provide the transmission coefficients needed for the calculation of the conductance. The calculated I-V curve agrees very well in shape with the measured result but, surprisingly, predicts more than two orders of magnitude larger current than is observed experimentally. A modification of the bonding configuration between the molecule and the electrodes, as shown at the right above, reduces the calculated current by about a factor of 25. The origin of the effect is the formation of a sigma bond between the p orbital of the sulfur and the s-orbital of the gold atom, which breaks the chain of pi-bonding states important in the conductance.

Clearly the atomic details of the molecular contact to the electrodes are crucially important in determining the properties of the junction.

Thus, in general, there are two separate portions of the device system that need characterization and structure/function relationships established. The first is the contacts, and the second is the nature of the molecules in the nano-scale device. Below we present methods that will aid in characterizing both of these parts of a molecular electronic device assembly.



Diagnostics of Molecular Devices

- Given difficulties in controlling the molecule/electrode interface, interpretation of measured I-V characteristics of molecular electronics device candidates would seriously benefit from experimental verification of molecular structure in the junction
- Tunneling spectroscopy of molecules in a Metal-Insulator-Metal junction is a classical technique (Jaklevic 1966), which can be used to provide the most useful molecular diagnostic, a vibrational spectrum

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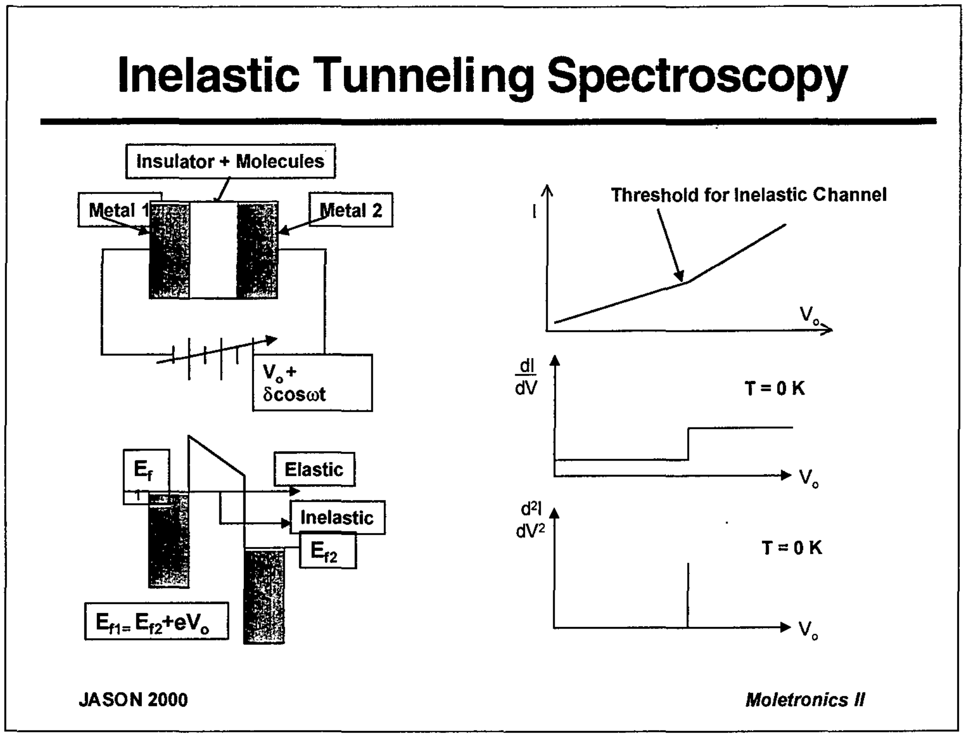
II.B. 6 Diagnostics for Molecular Devices

We now turn to methods for characterizing the actual state of the molecule that is in the gap between two very small metallic contacts.

A key research problem in developing molecular electronic devices is developing controlled approaches to trapping molecules between electrodes. Molecular arrays, often in the form of self-assembled monolayers (SAMs), have been used for this purpose. Measurements of the properties of individual molecules have used break junctions or STM tip probes. In all cases, controlling the contact between the molecule and the electrode is a crucial issue. Even if the molecule is cleanly bonded to the electrode, the structure of the electrode atoms at the junction can change the conductivity of the junction dramatically. In the more common case, where the nature of the bond between the molecule and at least one of the electrodes is poorly understood, then interpreting the measured I-V curves in terms of an idealized model is not straightforward because interfacial barriers (e.g. analogous to Schottky barriers) can effect the observed tunneling characteristics. The additional issues of trapped charge states and non-uniform density of states at either of the electrodes can also introduce dramatic new features, as discussed previously.

Characterization of molecular structure in tunnel junctions, by measurement of vibrational spectra, can be performed by the classical technique of Inelastic Tunneling Spectroscopy (IETS).

See:
J. Lambe and R. Jaklevic, Phys. Rev. Lett 17, 1139 (1966), and R.C. Jaklevic, Ch. 15,; P.K. Hansma, Ch. 1, in *Tunneling Spectroscopy Capabilities, Applications and New Techniques*, Ed. P.K. Hansma (Plenum, NY 1982).



Inelastic Tunneling Spectroscopy

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Moletronics II

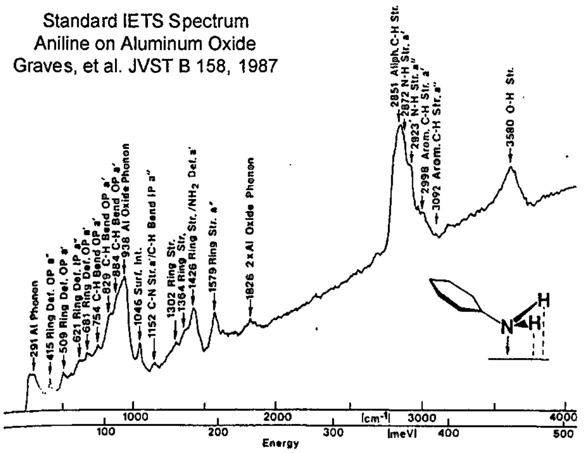
II.B. 6 Diagnostics for Molecular Devices

Traditionally, Inelastic Tunneling Spectrocopy (IETS) is performed in a parallel plate configuration, in which one metal electrode is oxidized to form an insulating barrier, typically 20-30 Å thick. The species of interest is deposited onto the oxide, and then the second electrode (often Pb) is evaporated on top.

Inelastic losses due to vibrational transitions are detected by sweeping the relative voltage of the two electrodes with an applied modulation. If the density of states, DOS, of the two electrodes is smooth, the tunneling current increases smoothly as the voltage between the electrodes increases. However, a discontinuity in the IV curve will occur if the tunneling electrons have the appropriate energy to excite vibrational transitions in the molecular species in the gap. This will occur when the voltage difference ΔV between the two electrodes becomes large enough (vibrational energy spacings are typically from 0 - 500 meV) to allow an electron emitted from the Fermi level of metal 1 to lose $e\Delta V$ of energy and still reach the unfilled states of the second electrode. Detection at the modulation frequency allows the second derivative of the tunneling current to be measured, showing the positions of the loss features clearly.

Spectra are measured at low temperature (4.2K) to prevent loss of signal intensity due to thermal broadening. Both IR and Raman active modes are observable in IETS, and, depending on the electrode material, demonstrate that even complex organic molecules can survive electrode deposition with little change from their structure in solution or gas phase.

Inelastic Tunneling Spectroscopy


Standard IETS Spectrum
Aniline on Aluminum Oxide
Graves, et al. JVST B 158, 1987

- Subtle changes in configuration and bonding of complex organics can be detected through vibrational spectrum

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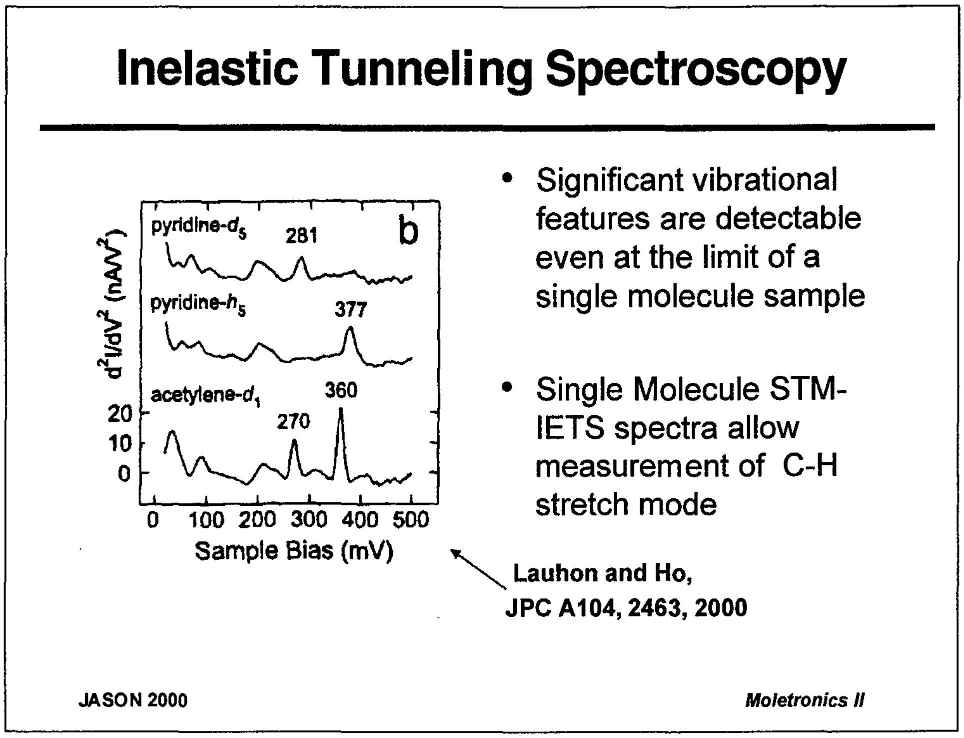
II.B. 6 Diagnostics for Molecular Devices

Studies of different electrode materials made during the development of IETS as an analytical technique showed that some metals, particularly some transition metals, caused serious changes in the vibrational spectra of the molecules deposited in the junction. This suggests that considerable caution should be exercised in designing molecular electronics junctions based on an evaporated second electrode.

Properly chosen electrodes, however, leave the vibrational spectra of molecules intact, with effects no more serious than peaks shifts of a few wavenumbers. The IETS spectrum thus can serve as a standard analytical "fingerprint" for the molecule in the junction. In addition to providing information about the molecular structure, the low-energy frustrated translational and rotational modes will be particularly valuable in characterizing the nature of the bonding to the electrodes.

Finally, it is useful that a wealth of information on molecular I-V properties already exists in the IETS literature. These data ought to provide a good reference point for choice of systems with interesting electronic properties.



Inelastic Tunneling Spectroscopy

- Significant vibrational features are detectable even at the limit of a single molecule sample
- Single Molecule STM-IETS spectra allow measurement of C-H stretch mode

Lauhon and Ho,
JPC A104, 2463, 2000

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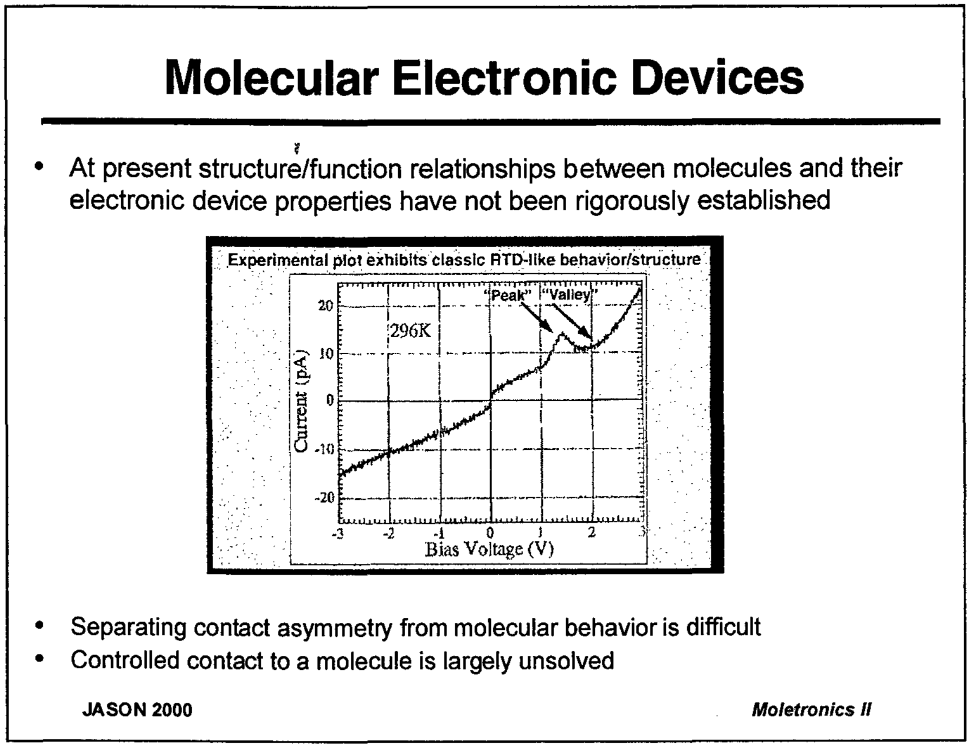
II.B.6 Diagnostics for Molecular Devices

IETS has excellent sensitivity to low densities of molecular species in the junction. In the parallel plate geometry, detection at the 0.01 monolayer level is readily achievable. In addition, the extension of IETS to the detectability limit of a single molecule has been demonstrated using an STM configuration. Remarkably, strong C-H stretch modes of organic adsorbates are clearly measurable, making this a feasible diagnostic approach for molecular devices.

See

B.C. Stipe, M. A. Rezaei, and W. Ho, Science 280 1732 (1998)

B.C. Stipe, M. A. Rezaei, and W.H. Ho, Rev. Sci. Inst. 70, 137 (1999).



Molecular Electronic Devices

- At present structure/function relationships between molecules and their electronic device properties have not been rigorously established

Experimental plot exhibits classic RTD-like behavior/structure

- Separating contact asymmetry from molecular behavior is difficult
- Controlled contact to a molecule is largely unsolved

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II.B.6 Diagnostics for Molecular Devices

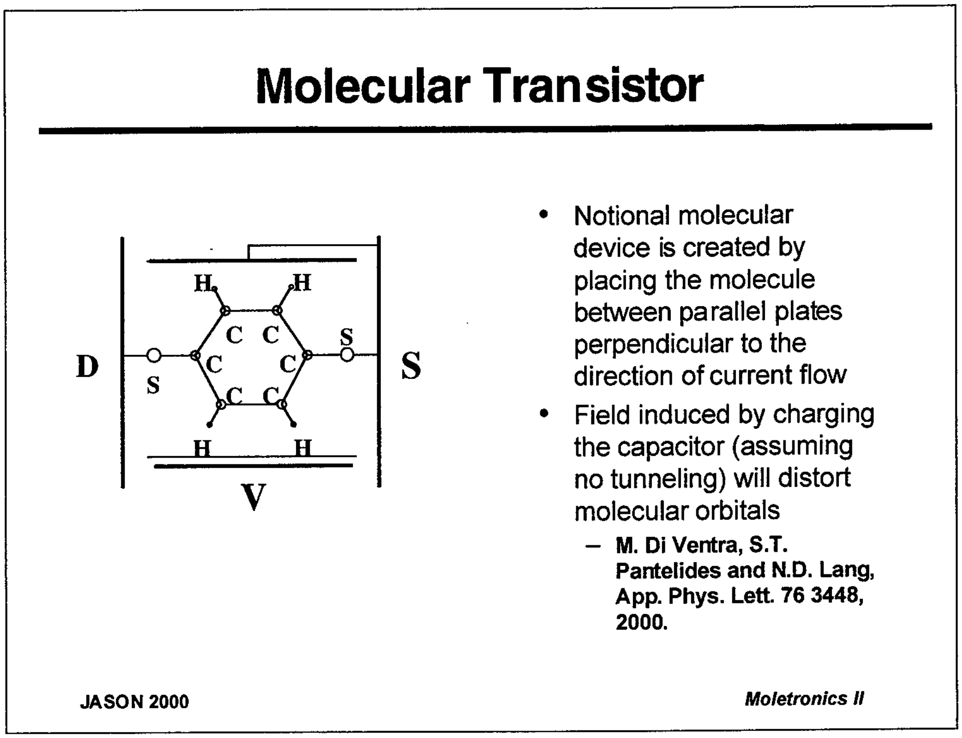
It would be appropriate to perform a systematic series of experiments that links the structure of the molecular system to its electrical properties. Important components of such a program include:

a) Characterization and control of the effects of contacts between the molecules and electrodes. This includes recognizing and using the molecular symmetry properties to distinguish IV characterizatics due to non-uniform contacts.

A device having symmetrical contacts should be used to contact a symmetrical molecule. The I-V curve ought to then be symmetrical with respect to applied voltage.

b) Systematically changing the molecular functionality using the powerful structure-function approach of organic chemistry. Specifically, the energy and spatial location of the relevant orbitals in the molecule should be varied and the device properties correlated with such variation.

c) The I-V properties should be correlated with theory and with measurements of the molecular orbital structure as probed both by electrochemical and by photoelectron spectroscopy data. Making such correlations will require including the effects of image charges on the energy levels for molecules between two metal contacts and corrections for the lack of solvation of the molecules in the device structure relative to the energy levels of the molecules in solution-based electrochemical measurements.



Molecular Transistor

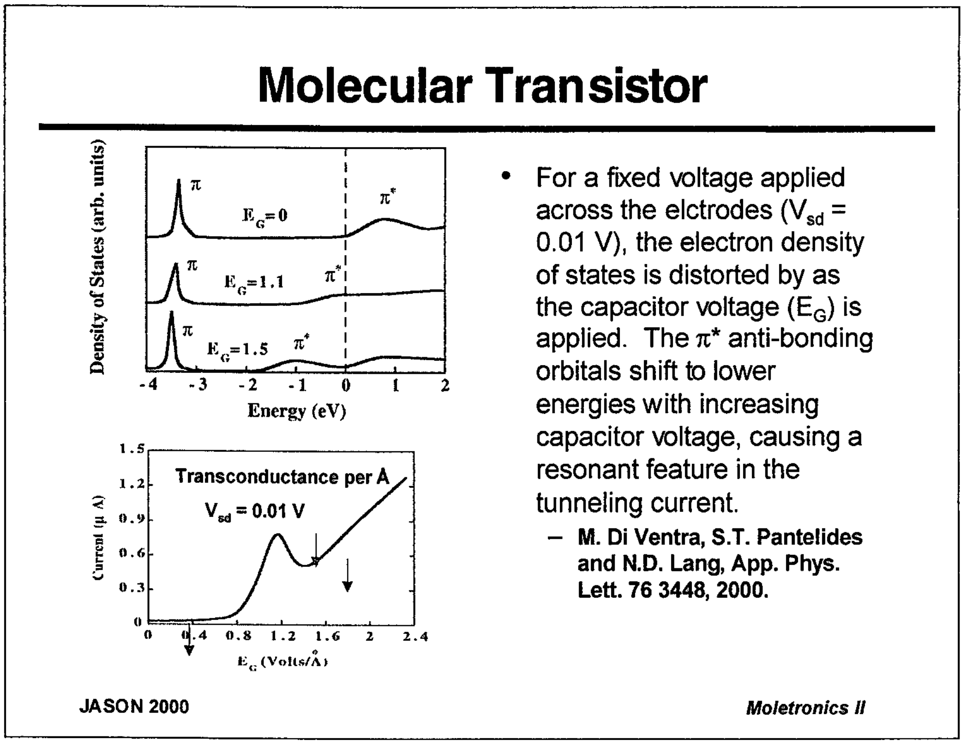
- Notional molecular device is created by placing the molecule between parallel plates perpendicular to the direction of current flow
- Field induced by charging the capacitor (assuming no tunneling) will distort molecular orbitals
  - **M. Di Ventra, S.T. Pantelides and N.D. Lang, App. Phys. Lett. 76 3448, 2000.**

II.B.7 Notional Molecular Transistor

It is also useful to consider alternative approaches to constructing molecular devices based on a detailed understanding of their transport properties.

Di Ventra, Pantelides and Lang have demonstrated how a rigorous understanding of the effects of electric fields on molecular properties may be exploited to create new molecular devices. They have considered the possibility of applying a lateral field to the molecule in the junction, illustrated conceptually above by the insertion of a pair of capacitor plates.

M. Di Ventra, S.T. Pantelides and N.D. Lang, App. Phys. Lett. 76 3448, 2000



Molecular Transistor

- For a fixed voltage applied across the elctrodes (V_{sd} = 0.01 V), the electron density of states is distorted by as the capacitor voltage (E_G) is applied. The π* anti-bonding orbitals shift to lower energies with increasing capacitor voltage, causing a resonant feature in the tunneling current.
  - **M. Di Ventra, S.T. Pantelides and N.D. Lang, App. Phys. Lett. 76 3448, 2000.**

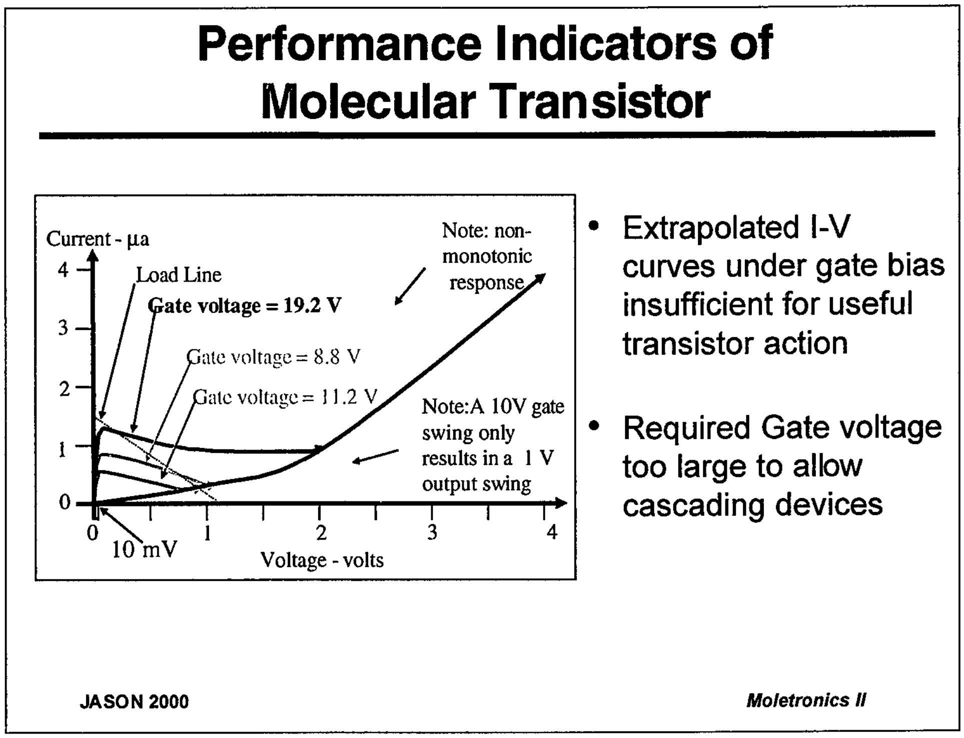
JASON 2000 ***Moletronics II***

II.B.7 Notional Molecular Transistor

Application of strong fields (the magnitudes are comparable to or larger than the fields applied between the tunneling electrodes) effectively causes a Stark shift of the π*-antibonding orbitals. When the applied bias between the electrodes is small, this shift brings the π* orbitals into alignment with the Fermi levels of the electrodes, causing enhanced conductivity. The predicted resistance at zero gate voltage is about 360 kohm, and drops close to the single-channel resistance of 12.9 kohm at a gate field of 1.1 V/Å, where the conductance reaches a maximum.

This demonstrates the possibility that molecular properties in a tunnel junction could be used to give transistor behavior. There are obviously difficulties in physical implementation. However, before that practical issue would need to be addressed, fundamental questions concerning the actual behavior of the transistor would still need to be resolved. Specifically, the fields needed to provide current control are large enough to cause a tunneling current to flow between the plates of the capacitor (e.g. in response to the gate voltage, defeating the purpose of a transistor). This problem (and the problem of molecular orientation with respect to the gate field) might be addressed by substantial modification of the molecular orbitals in the junction (e.g. via choice of the molecular conductor).

A second issue is the relative magnitude of the gate voltage and the source-drain voltage, as illustrated on the following page.



Performance Indicators of Molecular Transistor

- Extrapolated I-V curves under gate bias insufficient for useful transistor action
- Required Gate voltage too large to allow cascading devices

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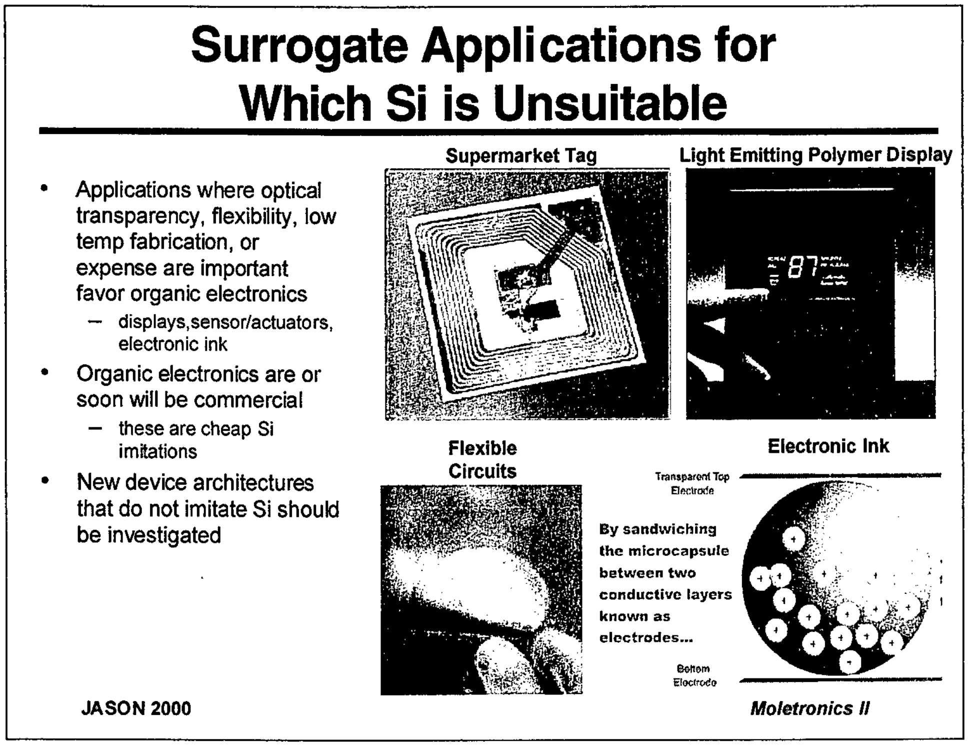
Moletronics II

II.B.7 Notional Molecular Transistor

The response curve shown on the previous page is the transconductance curve, the output (drain) current as a function of input (gate-to-serve) voltages, while held at a fixed source drain voltage. Standard performance of semiconductor-based transistors requires that in defining transistor device properties, it is necessary to know the transconductance at all source-drain voltages, so that the gate-voltage dependent series of I-V curves can be constructed. By extrapolating the information presented by DiVentra and co-workers for the shifts due to the source-drain voltage, an estimate of this information can be made for the benzene-thiol molecular transistor, as shown above. Because the source-drain and the gate voltages shift the positions of the π^* orbitals in opposite directions, it seems unlikely that this molecular transistor would provide a montonically increasing I-V response at fixed gate voltage. Thus, use of such a molecular transistor would require developing a new circuit design suited to the real properties of molecules, rather than those of silicon. (Alternatively, research on other molecular conductors could discover molecules with more "silicon-like" device behavior.)

Finally, we note that standard silicon-based circuit design typically uses transistors in a cascade configuration, that is, one in which the source or drain of one transistor is used to drive the gate of another. This would not be possible with the notional molecular transistor discussed above, because the peak of the tranconductance curve (at a gate field of 1.1 V/Å) occurs at a much higher voltage than the 0.010 V of the source-drain output.



Surrogate Applications for Which Si is Unsuitable

- Applications where optical transparency, flexibility, low temp fabrication, or expense are important favor organic electronics
  - displays,sensor/actuators, electronic ink
- Organic electronics are or soon will be commercial
  - these are cheap Si imitations
- New device architectures that do not imitate Si should be investigated

Supermarket Tag

Light Emitting Polymer Display

Flexible Circuits

Electronic Ink

Transparent Top Electrode

By sandwiching the microcapsule between two conductive layers known as electrodes...

Bottom Electrode

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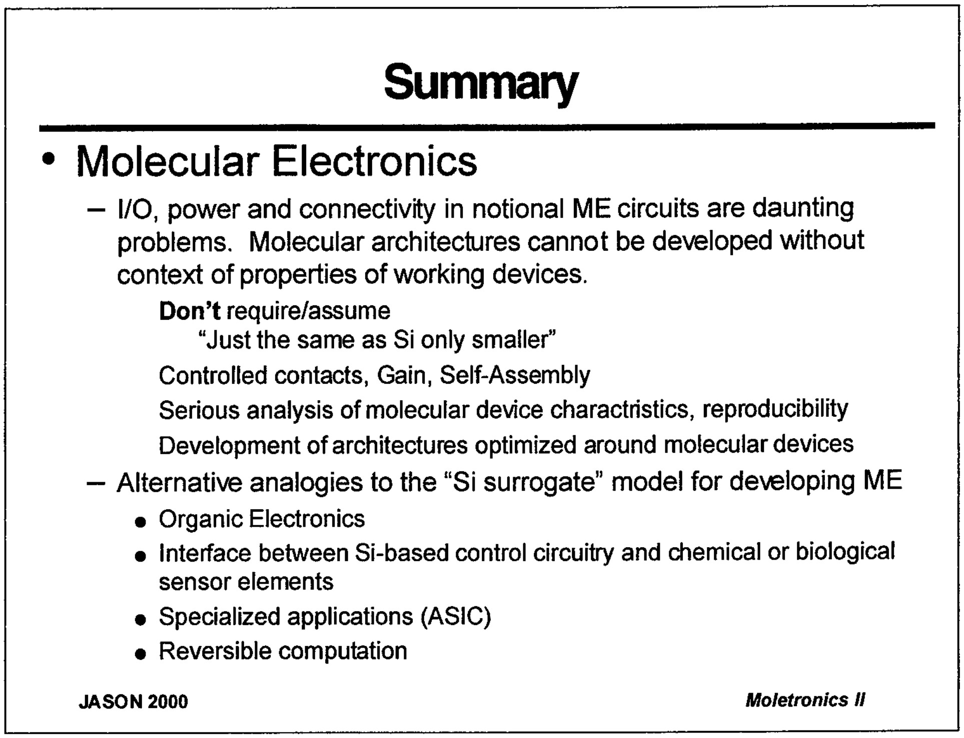
Moletronics II

II.C. Models from Organic Electronics

There are a number of niches where organic electronics has significant advantages over Si. In general, organic electronics offer great promise in applications where at least one of the following is important: expense, expense/area, transparency, mechanical flexibility or deformability, or compatibility with materials such as plastics that do not tolerate high temperatures.

Simple and inexpensive fabrication using printing processes at room temperature suggest that organic electronics will open up applications for which use of Si is too expensive. In addition, the compatibility of organic electronics with plastic substrates should encourage the fabrication of devices that are transparent and/or flexible. Applications involving combinations of sensors and actuators in visual or fluidic systems offer particular promise. Such systems may be massively parallel and may not require the same level of reliability and accuracy as is needed in computer CPU's, for example.

Organic electronics are already less expensive to fabricate than amorphous silicon, and p-type materials, such as pentacene, can have mobilities as high as 1.5 cm^2/V-s which is about twice the mobility of amorphous Si. N-type materials are less well developed, but the Bell Labs material “F15” is stable and soluble at room temperature. Circuits made from the material can be fabricated by a straightforward printing process. At present, the feature sizes of organic electronics are of the order of 100 microns, and the speeds are of the order of 10 kilohertz.



Summary

- Molecular Electronics
  - I/O, power and connectivity in notional ME circuits are daunting problems. Molecular architectures cannot be developed without context of properties of working devices.
    - **Don't** require/assume "Just the same as Si only smaller"
    - Controlled contacts, Gain, Self-Assembly
    - Serious analysis of molecular device charactristics, reproducibility
    - Development of architectures optimized around molecular devices
  - Alternative analogies to the "Si surrogate" model for developing ME
    - Organic Electronics
    - Interface between Si-based control circuitry and chemical or biological sensor elements
    - Specialized applications (ASIC)
    - Reversible computation

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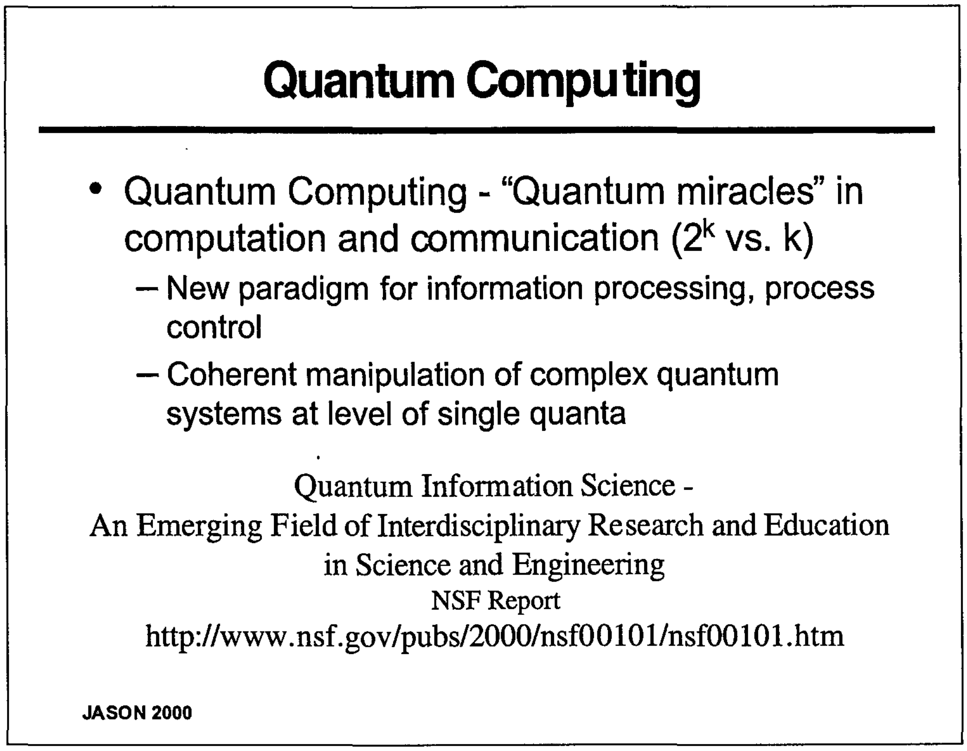
II.D. Molectronics Summary/Recommendations

The research area known as molecular electronics has recently shown rapid development due to advances in structural and electronic characterization capabilities at the level of individual molecules. Popular reports have emphasized the potential for the development of molecular computers, with dreams that self assembly will cut production costs, and size scaling will ultimately allow the limits of Si-based computing to be surpassed. We have reviewed the issues involved in developing molecular-based information technology analogous to present-day Si-based technology. Fairly simple analysis shows that performance limiters such as power dissipation, interconnect density and data transfer rate will not scale linearly with size, so that size scaling arguments for improved performance in molecular electronics must be critically evaluated. The state-of-the art results in molecular electronic performance were also evaluated. It is clear that the ability to fabricate molecular devices is now at a basic research level, where continued discovery and careful quantification are needed to advance the field.

Discussions of molecular electronics architectures have relied on analogies between molecular and standard electronic components (e.g. resistor, conductors, diodes...). We have presented an overview of how real molecular device properties differ from those of standard electronic components. Because of these differences, we believe that a focus on developing molecular circuitry based on analogies to Si-based computer architecture is not appropriate. Instead, serious understanding of molecular electronics properties, and a correlated development of molecular architectures that work because of (rather than despite) special molecular characteristics, is needed for real progress toward the goal of practical molecular electronic technologies.



Quantum Computing

- Quantum Computing - "Quantum miracles" in computation and communication (2^k vs. k)
  - New paradigm for information processing, process control
  - Coherent manipulation of complex quantum systems at level of single quanta

Quantum Information Science -
An Emerging Field of Interdisciplinary Research and Education
in Science and Engineering
NSF Report
http://www.nsf.gov/pubs/2000/nsf00101/nsf00101.htm

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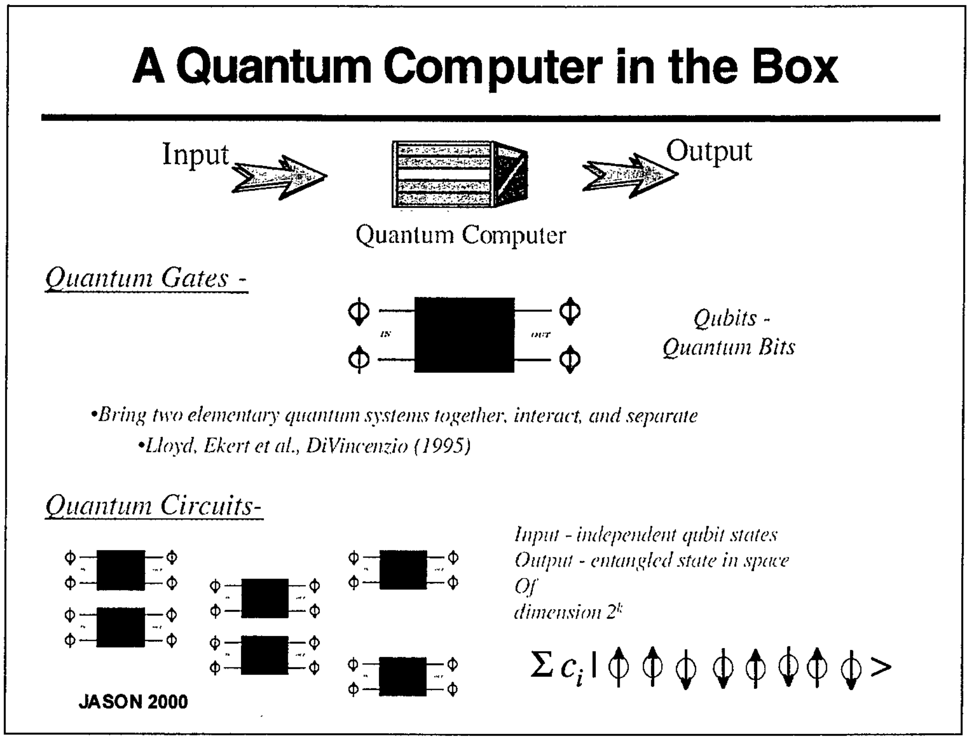
III. QUANTUM COMPUTING

The "big win" of quantum computation is the ability to access exponential resources (the Hilbert space of dimension 2^k) with physical k qubits. Of course, the catch is that one has to be very clever in order to utilize this big space because of the constraints imposed by quantum measurement (i.e., only one of the 2^k possibilities is actually accessed when the state is measured.



A Quantum Computer in the Box

Quantum Gates -

Qubits -
Quantum Bits

- *Bring two elementary quantum systems together, interact, and separate*
  - *Lloyd, Ekert et al., DiVincenzio (1995)*

Quantum Circuits-

Input - independent qubit states
Output - entangled state in space
Of
dimension 2^k

$$\Sigma c_i \,|\, \uparrow\uparrow\downarrow\downarrow\uparrow\downarrow\uparrow\downarrow >$$

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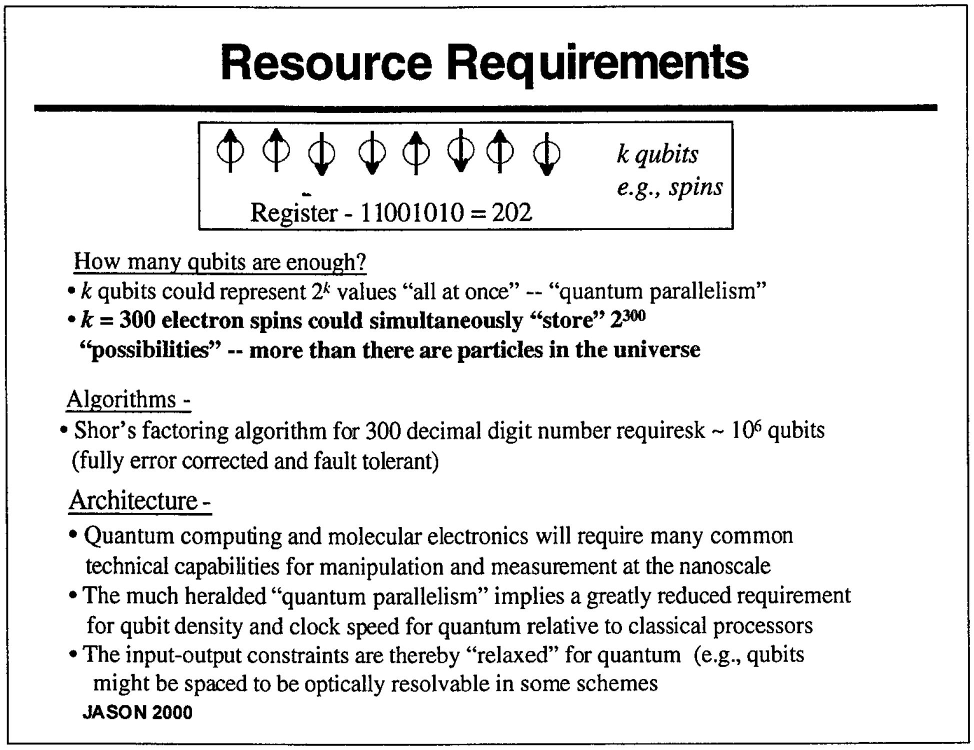
III.A. Basic Problem Approach

Shor's algorithms for factoring and discrete log are the spectular examples of an exponential win made possible via quantum computation. The tremendous interest in these otherwise esoteric examples arises from the fact that public key crypto-systems rely upon the computational difficulty of factoring and discrete log, both of which become computationally "easy" on a quantum computer.

The second example of an exponential win is simulating quantum evolution by a quantum computer, which may ultimately be important for the development of quantum technologies.

The fact that one anticipates exponential wins for quantum computers means that such machines do not have to be built with moles of bits and do not have to operate at tera-Hertz speeds.



Resource Requirements

k qubits
e.g., spins

Register - 11001010 = 202

How many qubits are enough?

- k qubits could represent 2^k values "all at once" -- "quantum parallelism"
- **k = 300 electron spins could simultaneously "store" 2^{300} "possibilities" -- more than there are particles in the universe**

Algorithms -

- Shor's factoring algorithm for 300 decimal digit number requiresk ~ 10^6 qubits (fully error corrected and fault tolerant)

Architecture -

- Quantum computing and molecular electronics will require many common technical capabilities for manipulation and measurement at the nanoscale
- The much heralded "quantum parallelism" implies a greatly reduced requirement for qubit density and clock speed for quantum relative to classical processors
- The input-output constraints are thereby "relaxed" for quantum (e.g., qubits might be spaced to be optically resolvable in some schemes

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•Requirements for factoring (assuming no errors and perfect gates) -

To factor a number with 300 decimal digits on a quantum computer via Shor's algorithm requires about 3000 qubits and 10^{10} operations

Example -

Classical computer

A 130 digit number was recently decomposed into its prime factors in 1 month. Using the same computational resources, a 400 digit number would take 10 billion years.

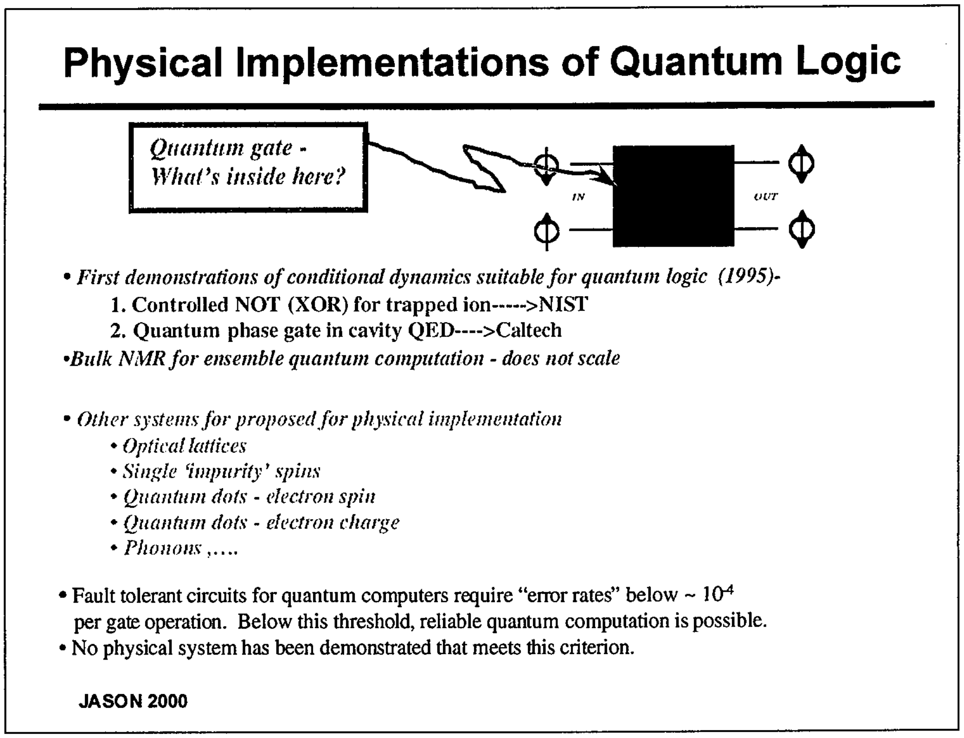
Quantum computer -

Assuming the same clock speed as for the above classical case, then a 130 digit number would require 1 second to be factored on a quantum computer. A 400 digit number would require 30 seconds.

•Requirements for factoring (assuming errors and imperfect gates, via fault-tolerant architectures in previous viewgraph) -

Number of qubits up 100 times (so 3 x10^3 qubits goes to 3 x10^5)

Number of operations up 100 times (so 10^{10} ops goes to 10^{12})



Physical Implementations of Quantum Logic

Quantum gate -
What's inside here?

- *First demonstrations of conditional dynamics suitable for quantum logic (1995)-*
  1. Controlled NOT (XOR) for trapped ion----->NIST
  2. Quantum phase gate in cavity QED---->Caltech
- *Bulk NMR for ensemble quantum computation - does not scale*

- *Other systems for proposed for physical implementation*
  - *Optical lattices*
  - *Single 'impurity' spins*
  - *Quantum dots - electron spin*
  - *Quantum dots - electron charge*
  - *Phonons ,....*

- Fault tolerant circuits for quantum computers require "error rates" below ~ 10^{-4} per gate operation. Below this threshold, reliable quantum computation is possible.
- No physical system has been demonstrated that meets this criterion.

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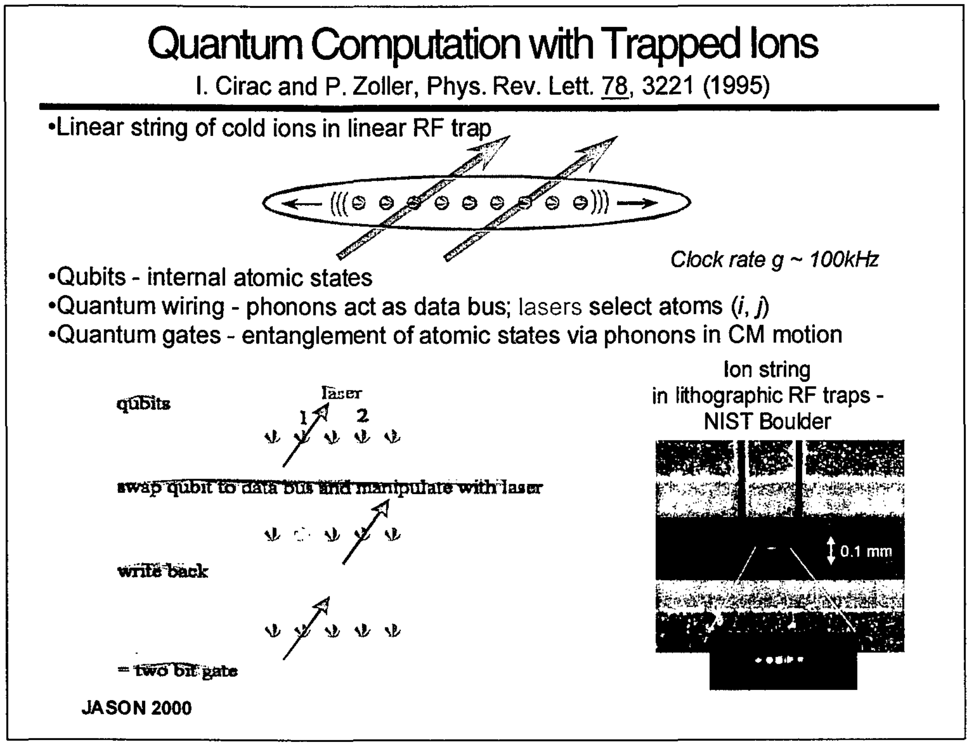
III.B. Research on Physical Implementation

Implementation of quantum computing requires "quantum wiring" among the q-bits and a means of initializing and reading the results of the computation.



Quantum Computation with Trapped Ions

I. Cirac and P. Zoller, Phys. Rev. Lett. 78, 3221 (1995)

- Linear string of cold ions in linear RF trap

Clock rate *g ~ 100kHz*

- Qubits - internal atomic states
- Quantum wiring - phonons act as data bus; lasers select atoms (*i, j*)
- Quantum gates - entanglement of atomic states via phonons in CM motion

Ion string
in lithographic RF traps -
NIST Boulder

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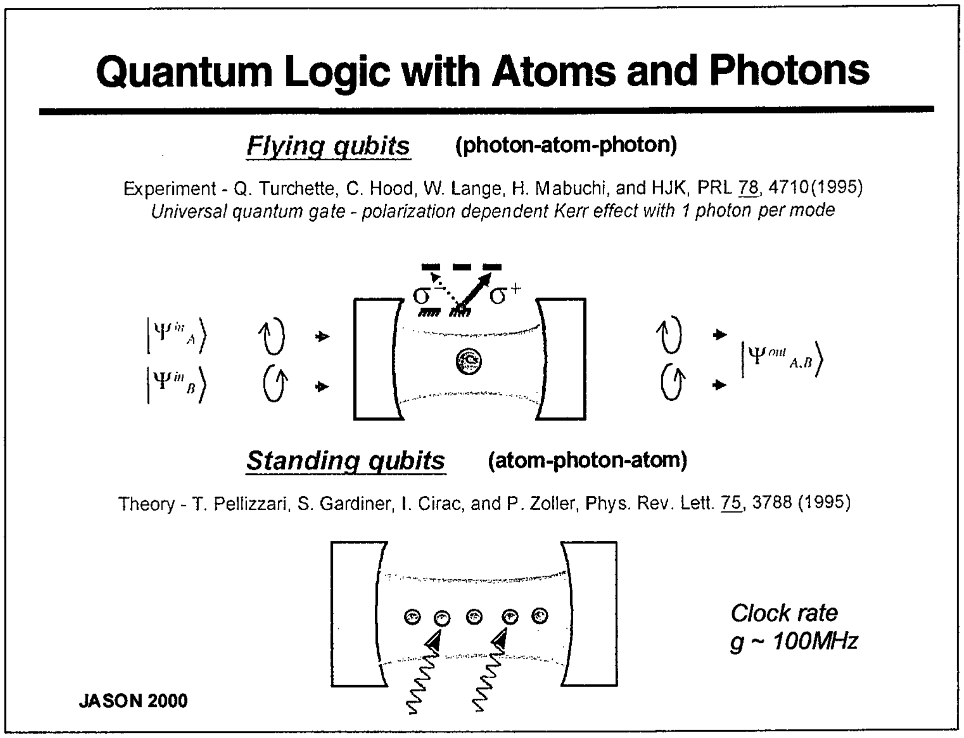
III.B. Research on Physical Implementation (Kimble)

Wiring - Collective mode of system - here, phonons in center-of-mass oscillation

Input/Output - Optically, via individually addressed ions ($^9Be^+$ in the picture above)

In 1995, NIST group carried out first demonstration of controlled-NOT gate (quantum XOR) for the implementation of quantum logic, between internal state of trapped ion and center-of-mass motion (phonon).

Most recently, spectacular demonstration of quantum logic operations on 4 qubits (ions) by the NIST Boulder group.



Quantum Logic with Atoms and Photons

Flying qubits **(photon-atom-photon)**

Experiment - Q. Turchette, C. Hood, W. Lange, H. Mabuchi, and HJK, PRL 78, 4710(1995)
Universal quantum gate - polarization dependent Kerr effect with 1 photon per mode

Standing qubits **(atom-photon-atom)**

Theory - T. Pellizzari, S. Gardiner, I. Cirac, and P. Zoller, Phys. Rev. Lett. 75, 3788 (1995)

Clock rate
g ~ 100MHz

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III.B. Research on Physical Implementation

- In the first instance, polarization states of single photons are the quantum bits (or qubits). Nonlinear interactions between photons as required for quantum logic can be mediated by single atoms in cavities.

- In 1995 the Caltech group carried out the first demonstration of conditional quantum dynamics at the single photon level suitable for the implementation of quantum logic. The basic mechanism employed was the polarization-dependent Kerr effect at the level of 1 photon/mode.

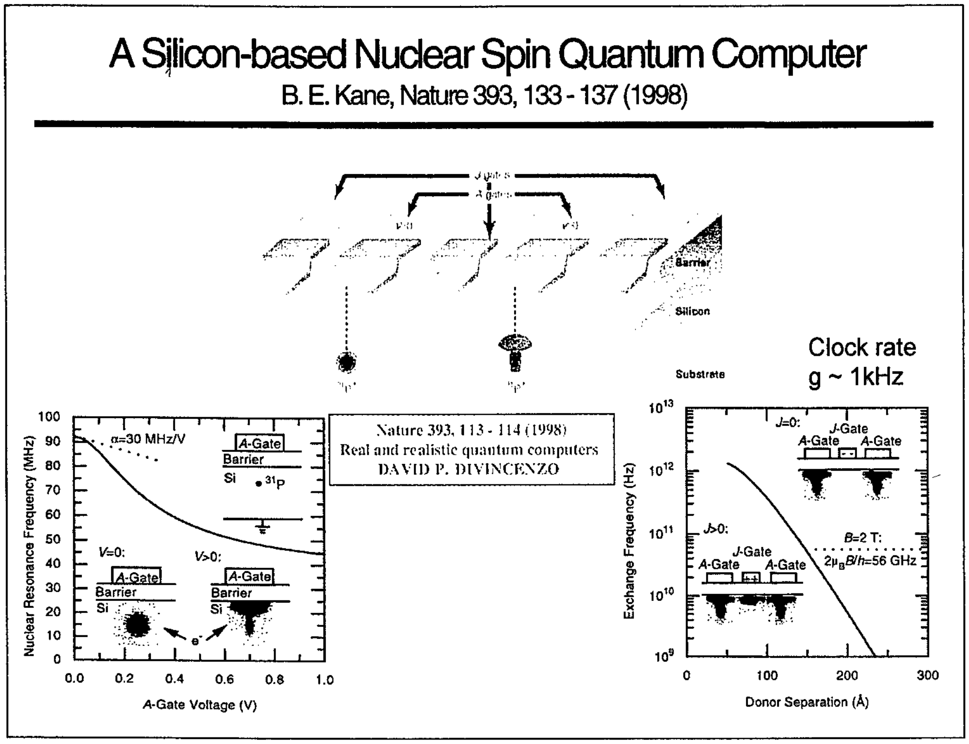
- Another possibility for quantum logic with single atoms and photons has been suggested and analyzed by Professors Peter Zoller and Ignasico Cirac and colleagues in Innsbruck. Here internal atomic states become qubits, with interactions now mediated by single photons. This second possibility is yet to be demonstrated in the lab.

Wiring - Collective mode of system - here, photons in intracavity field

Input/Output - Optically, via individually addressed atoms

Required capabilities - trapping of single atoms in high-quality optical cavities (initial demonstrations), generation of single photon states (yet to be done), controlled transfer from atom to photon to atom (yet to be accomplished).

Extensions to single atoms in photonic bandgap cavities, quantum dots in optical cavities have been proposed, and are under experimental investigation.



A Silicon-based Nuclear Spin Quantum Computer

B. E. Kane, Nature 393, 133 - 137 (1998)

Clock rate
g ~ 1kHz

Nature 393, 113 - 114 (1998)
Real and realistic quantum computers
DAVID P. DIVINCENZO

III.B. Research on Physical Implementation

Qubits in this case are nuclear spins of individual ^{31}P atoms doped into silicon.

A gate - loosely bound electron of ^{31}P atom can be polarized, changing the overlap with the nucleus. Since interaction of electron and nucleus determines energies of nuclear spin states, the spin of an individual ^{31}P atom can thereby be addressed by a combination of external microwave field and voltage on A gate.

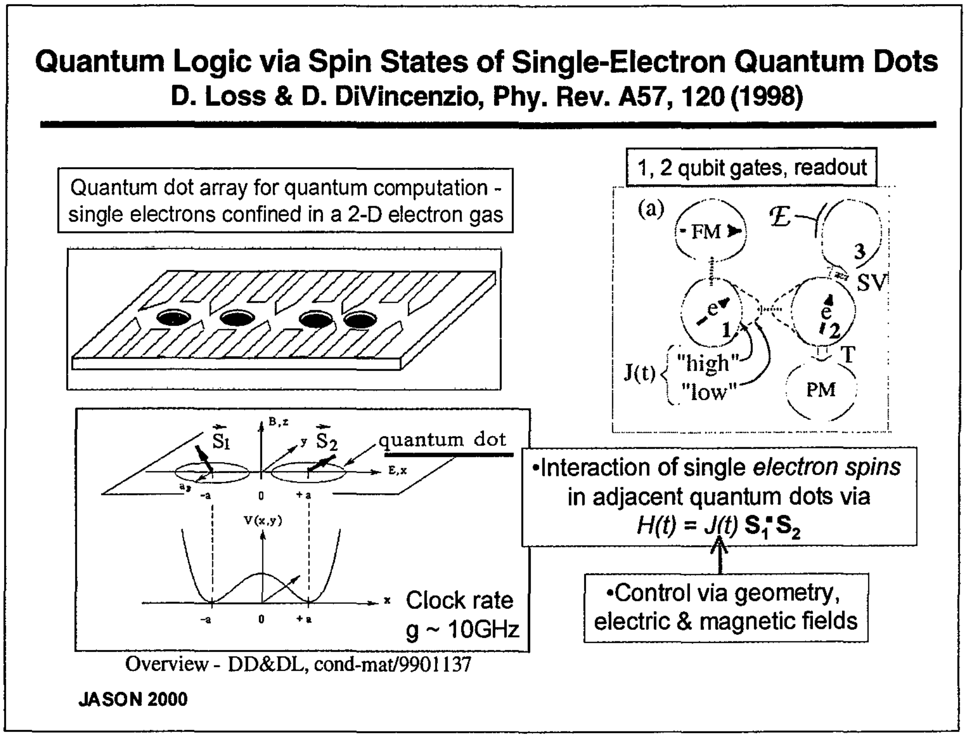
J gate - controls overlap of neighboring electrons, which mediate coupling between ^{31}P nuclear spins. Voltages on J gates thus provide for two-qubit interactions (gates).

Wiring - Pair-wise interactions taken one after the other allow two remotely located ^{31}P atoms to interact.

Input/Output - Via a series of interactions to convert nuclear spin to electron charge. First, select a particular ^{31}P atom via A gate. A large swing of the J-gate voltage then causes the electron from the neighboring ^{31}P atom to hop to the selected site conditioned upon whether or not the nuclear spin of the atom selected by the A gate is up or down. In one case, the ^{31}P atom selected by the A gate gets two electrons, and in the other not, with these two cases then read out by measuring the capacitance between the neighboring A electrodes

Doping and detection of single ^{31}P atoms yet to be accomplished.

Requisite interactions and measurements capabilities for A/J gates have yet to be demonstrated.



Quantum Logic via Spin States of Single-Electron Quantum Dots

D. Loss & D. DiVincenzio, Phy. Rev. A57, 120 (1998)

Quantum dot array for quantum computation - single electrons confined in a 2-D electron gas

1, 2 qubit gates, readout

- Interaction of single *electron spins* in adjacent quantum dots via $H(t) = J(t)\,\mathbf{S}_1 \cdot \mathbf{S}_2$

- Control via geometry, electric & magnetic fields

Clock rate
g ~ 10GHz

Overview - DD&DL, cond-mat/9901137

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III.B. Research on Physical Implementation

Qubits here are electron spins (single electrons confined in 2-D electron gas)

2-qubit interactions controlled via electrodes. Raise or lower tunnel barrier via gate voltage to change $J(t)$ and hence mediate interaction between neighboring spins.

Wiring - Pair wise interactions between electron spins (hand shake down the chain)

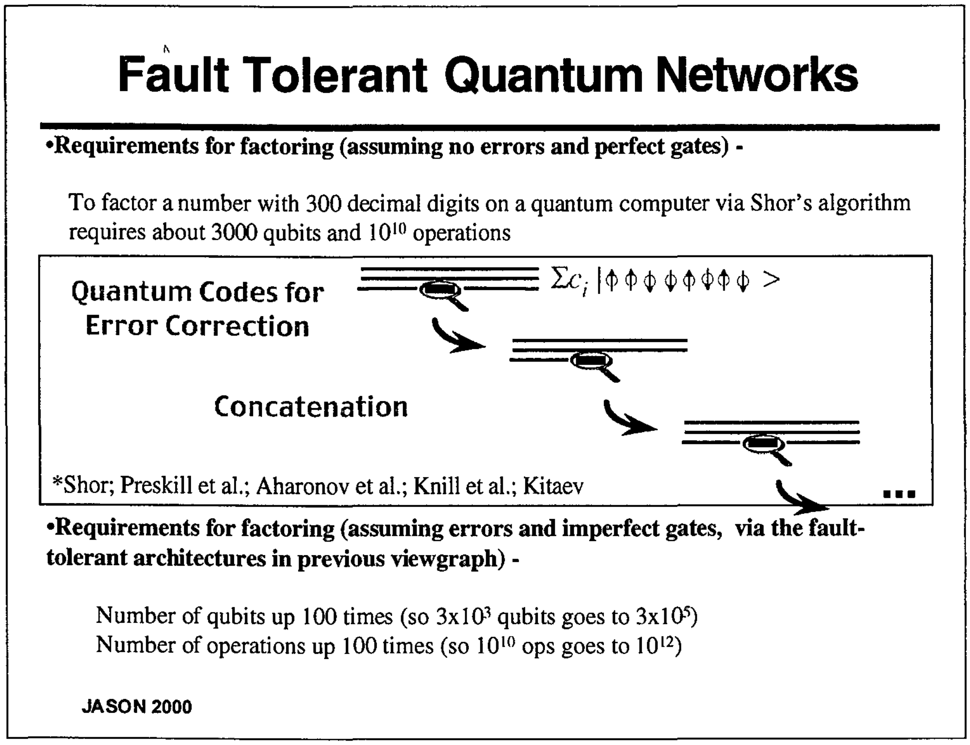
Input/Output -

FM - Ferromagnetic dot. Electrical gating provides for single qubit gate. Raise or lower barrier between electron and FM, with then the single electron spin (the qubit) polarized by way of its interaction with the ferromagnetic domain.

PM - Paramagnetic dot. Electrical gating of interaction causes the single qubit to nucleate a metastable phase of ferromagnet (hence, initial one spin polarizes many spins, which are then read somehow).

SV - Spin valve. Spin dependent tunneling converts electron spin to charge, which is then read via single electron transistor.

This implementation requires the development of magneto-electronic techniques (materials growth, detection techniques, ...)



Fault Tolerant Quantum Networks

•Requirements for factoring (assuming no errors and perfect gates) -

To factor a number with 300 decimal digits on a quantum computer via Shor's algorithm requires about 3000 qubits and 10^{10} operations

Quantum Codes for Error Correction $\Sigma c_i |\phi\phi\phi\phi\phi\phi\phi >$

Concatenation

*Shor; Preskill et al.; Aharonov et al.; Knill et al.; Kitaev

•Requirements for factoring (assuming errors and imperfect gates, via the fault-tolerant architectures in previous viewgraph) -

Number of qubits up 100 times (so $3\text{x}10^3$ qubits goes to $3\text{x}10^5$)
Number of operations up 100 times (so 10^{10} ops goes to 10^{12})

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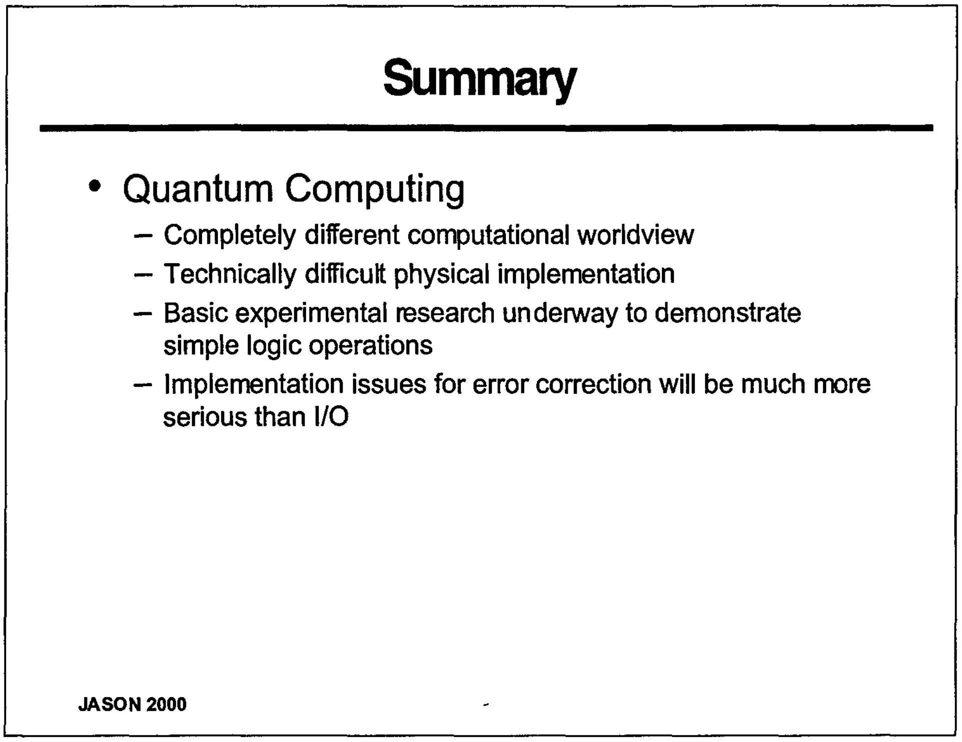
III.C. Error Correction

Quantum error correction involves encoding information from one logical qubit into several physical qubits (at least 5 are required, more popularly 7 qubits).

Concatenated coding then nests these quantum error correcting codes in successive layers. Not shown are associated "ancilla" qubits that must constantly be initialized, interact with the computational qubits and then read out. Conditioned upon the readout, actions must be taken to correct (or not) errors that might have occurred.

A great triumph of recent years is the discovery of a threshold for the convergence of these complicated protocols. If the error rate is below a certain level (roughly 10^{-4}), then essentially, the errors can be fixed faster than they occur. Large scale quantum coherence is then maintained across the whole quantum computer, and computations of indefinite length become possible.

However, it should be emphasized that there is a very wide gulf between the abstract fault tolerant architectures for a quantum computer and possible physical implementations (such as the previously discussed examples). No one really knows how to accomplish all of the requisite interactions and readouts in a given physical system.



Summary

- Quantum Computing
  - – Completely different computational worldview
  - – Technically difficult physical implementation
  - – Basic experimental research underway to demonstrate simple logic operations
  - – Implementation issues for error correction will be much more serious than I/O

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IV. QUANTUM COMPUTING SUMMARY/RECOMENDATIONS

Quantum information processing represents a new paradigm for computation and communication with potentially profound impact. The "big win" of quantum computation is the ability to access exponential resources (the Hilbert space of dimension 2^k) with physical k quantum bits ("qubits"). Of course, there are also "big problems," principal among them being that quantum measurement imposes severe constraints on the ability to extract information from the large state space and that quantum states are extremely sensitive to extraneous perturbations.

Several technologies for implementing Quantum Computing have been proposed, and demonstrations of prototype q-bits have been achieved. Both photon/trapped ion or atom systems, and solid-state systems are under investigation, and the research focus is well matched to the ultimate goals of technology development. Mastering the difficult technologies involved is a necessary, and enabling, first step toward the very difficult problem of assembling systems with the full complement of q-bits needed for real computation. The need to increase the number of q-bits and operations by at least 2 orders of magnitude to implement error correction is a well understood, major challenge in this long-term research effort.

APPENDIX A - Scaling Analysis

The lure of molecular electronics is of making circuit elements much smaller than is possible with conventional lithography, and of achieving much greater densities of information storage. Because smaller circuit elements may have shorter RC relaxation times and smaller carrier diffusion times in transistors, it is also hoped that molecular electronic devices will provide much faster rates of information processing. Here we consider some constraints on what can be achieved. The principles are essentially the same for silicon-based electronics and for novel molecular electronics, although the materials properties and fabrication difficulties differ.

We will in general consider circuit elements of dimensions $l \times l \times h$ where $l > h$ is a horizontal feature size and a h is a thickness. For molecular electronics $l \sim h \sim 30$ Å, while for conventional electronics $l >> h \sim 30$ Å. Obviously, this is an oversimplification of the dimensions of real devices, but some sort of oversimplification is necessary to make estimates independent of (presently unknown) details of specific technologies. We will take the dielectric constant of insulating layers to be equal to $\varepsilon = 4$, the value appropriate to SiO_2 although organic materials typically in fact have much lower dielectric constant, $\varepsilon \sim 1.5$. Capacitances are then

$$C \approx \frac{\varepsilon l^2}{h},$$

and resistances of conducting links

$$R \approx \frac{\rho}{h},$$

where ρ is the resistivity.

The relaxation time sets a lower bound on the switching and cycle times. The actual value of t depends on the conductivity of the circuit elements (including transistors, whose conductivity is much less than that of metallic wires, and probably much less than that of molecular conductors) and the diffusion time of carriers in transistors. It therefore depends on details of the specific materials and configurations. Simple estimates (for example, of RC times or carrier diffusion times) often lead to spectacularly short values. For example, the RC relaxation time for metallic conducting links

$$t_{RC} \sim \frac{l^2 \varepsilon \rho}{h^2}$$

is very short ($\sim 10^{-14}$ s for $l = 30\, h$). A transistor provides a modulatable resistance orders of magnitude higher, limited by the doping level and carrier mobility, whereas no general estimate is applicable to the entire class of hypothetical molecular electronic materials.

A second constraint is the carrier diffusion time, which limits the speed at which a transistor may be switched. These times are also very short:

$$t_{mobil} \sim \frac{l^2}{\mu V},$$

where V is the voltage and m the carrier mobility. For $l = 1000$ Å , $\mu = 1400$ cm^2/Volt-s (appropriate to electrons in Si) and $V = 1$ Volt, this produces $t_{\text{mobil}} = 10^{-13}$ s. Each of these times is reduced by a factor of 1000 on molecular scales, with $l = 30$ Å; although the appropriate values of ρ and μ are not known until the materials are specified.*

More stringent constraints arise, however, from power dissipation. A very simple estimate may be made by considering circuit elements on two surfaces that are located a distance h apart. Then, independent of the size of the circuit elements (which, however, cannot be less than h), the power dissipation per unit area P at a cycle rate ν is

$$P = \frac{1}{2} fV^2 \frac{\varepsilon}{h} \nu \sim \left(\frac{f}{0.01}\right)\left(\frac{V}{\text{Volts}}\right)^2 \left(\frac{30\,\text{Å}}{h}\right)\left(\frac{\nu}{10^9\,\text{Hz}}\right) 70\,\text{W/cm}^2$$

where the duty factor f reflects the fraction of the area actually covered with capacitive energy storage and the fraction of these elements switched each cycle.

Reasonable power dissipations are ~ 100 W/cm^2. This depends somewhat on the materials and cooling mechanisms employed, but the value cannot be increased by an order of magnitude. Even with a very heat-resistant and conductive semiconductor, such as diamond, the problem remains of removing heat from the diamond. It is therefore evident that ν cannot be increased much over present values of ~ 10^9 s^{-1} unless f is very small. Thus, very fast circuit elements can only be accessed infrequently. This may be satisfactory for memory elements, which may be quasi-archival, but it is unlikely to be satisfactory for processors. We do note, however, that if processors are interspersed with memory on a single chip, lateral heat diffusion in the chip itself (especially if it is a good thermal conductor) may make the relevant criterion the mean thermal load averaged over both the frequently-switched processor elements and the infrequently-switched memory elements.

A volatile memory element must dissipate at least $q\, k_B T$ each relaxation time (*N.B.* : transistors with high resistivity in the nonconducting state make the relaxation time quite long when they are not being switched). The factor q comes from the requirement that the probability of a spontaneous error caused by thermal excitation be acceptably low:

$$q = \ln\left(\frac{\nu NA}{\text{AER}}\right)$$

---

[*] It must be re-emphasized here, as in the text, that such scaling analysis only will work if the molecular transport mechanism is the same as for standard devices. Otherwise the governing equations will be different.

where N is the number of memory elements, A the device lifetime and AER the acceptable probability of a single error anywhere in the device during that lifetime. Numerical evaluation leads to $50 < q < 100$ for any reasonable assumptions; we will adopt $q = 100$.

The assumption of a thermal noise bound on the error rate may be suspect. It is possible that in real devices nonthermal excitation will produce a higher error rate. This cannot be estimated through the use of general principles alone. However, as circuit elements become smaller the signals available for excitation by cross-talk become smaller. If there is a threat of nonthermal errors it probably comes from coherent external transients (which may be shielded) rather than cross-talk among neighboring circuit elements.
This requirement sets a lower bound on the size of capacitive elements, because they must store at least $q\, k_B\, T$ of energy:

$$\frac{1}{2}CV^2 \approx \left(\frac{V}{\text{Volts}}\right)^2\left(\frac{C}{10^{-6}\text{cm}}\right)k_B 40,000°\text{K}$$

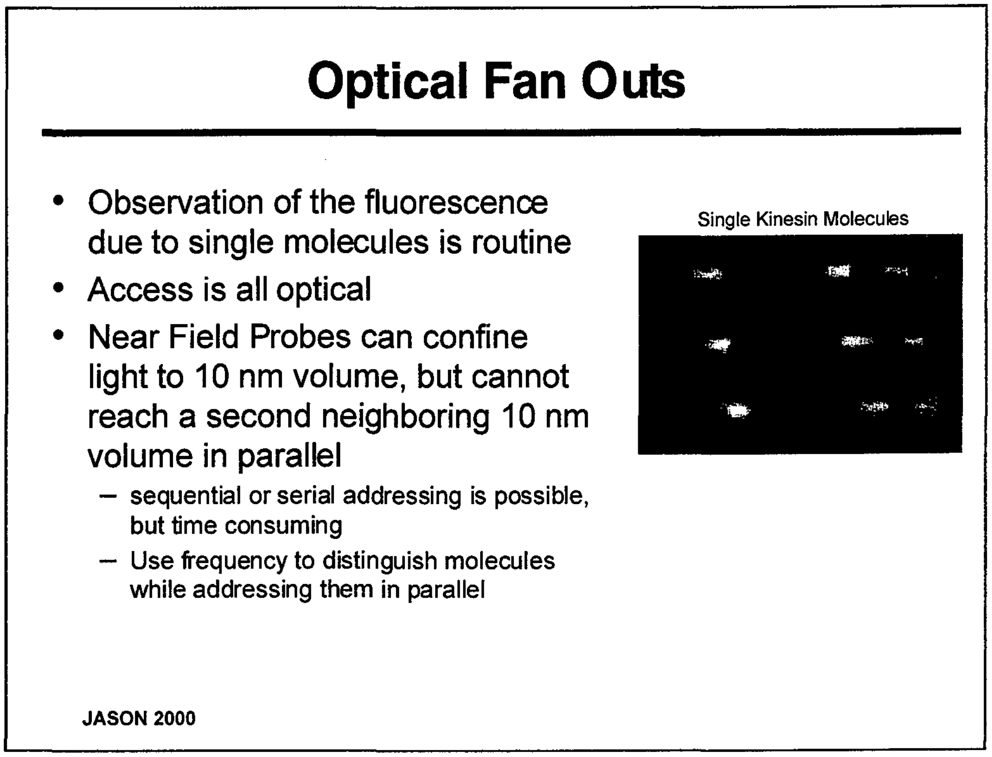
where a capacitance of 10^{-6} cm (cgs) is 1.1×10^{-18} farad. This is approximately the capactance of two conductors with $l \sim h \sim 30$ Å and $\varepsilon = 4$. Smaller h permits smaller $l \propto h^{1/2}$, but the dimensions of atoms mean that features much smaller than $l \sim h \sim 30$ Å are unlikely to be practical. Very large ε is found in bulk materials near ferroelectric transitions, but these values depend on domain wall motion and are not applicable to the nanoscales and high frequencies discussed here.

It is sometimes suggested that molecular electronics will necessarily operate at very low voltages (<< 1 V) in order to keep electric fields below breakdown thresholds. However, these thresholds are not applicable to fields applied over short distances. A total potential drop of 1 V cannot produce classical breakdown when the ionization threshold exceeds 1 eV, however large the local electric field. Analogous phenomena involving ionization of impurity states close to a conduction band may occur, but are part of a device's (potentially useful) electronic properties, not destructive breakdown.

In fact, there is an argument that potentials of molecular electronic devices are naturally a few Volts. If a capacitor stores an energy $q\, k_B\, T$ then its charge

$$Q = \frac{2qk_BT}{V} = \left(\frac{q}{100}\right)\left(\frac{5\text{Volts}}{V}\right)\left(\frac{T}{300°K}\right)e.$$

To minimize power consumption q should not much exceed 100. Then, if $V = 5$ volts the capacitor stores a single electron. There is a natural marriage between digital electronics and the discrete nature of single-electron electronics, and (at room temperature) it can only be consummated at these comparatively large voltages. Lower voltages may be possible in cryogenic operation, and would also reduce the power dissipation.



Optical Fan Outs

- Observation of the fluorescence due to single molecules is routine
- Access is all optical
- Near Field Probes can confine light to 10 nm volume, but cannot reach a second neighboring 10 nm volume in parallel
  - sequential or serial addressing is possible, but time consuming
  - Use frequency to distinguish molecules while addressing them in parallel

Single Kinesin Molecules

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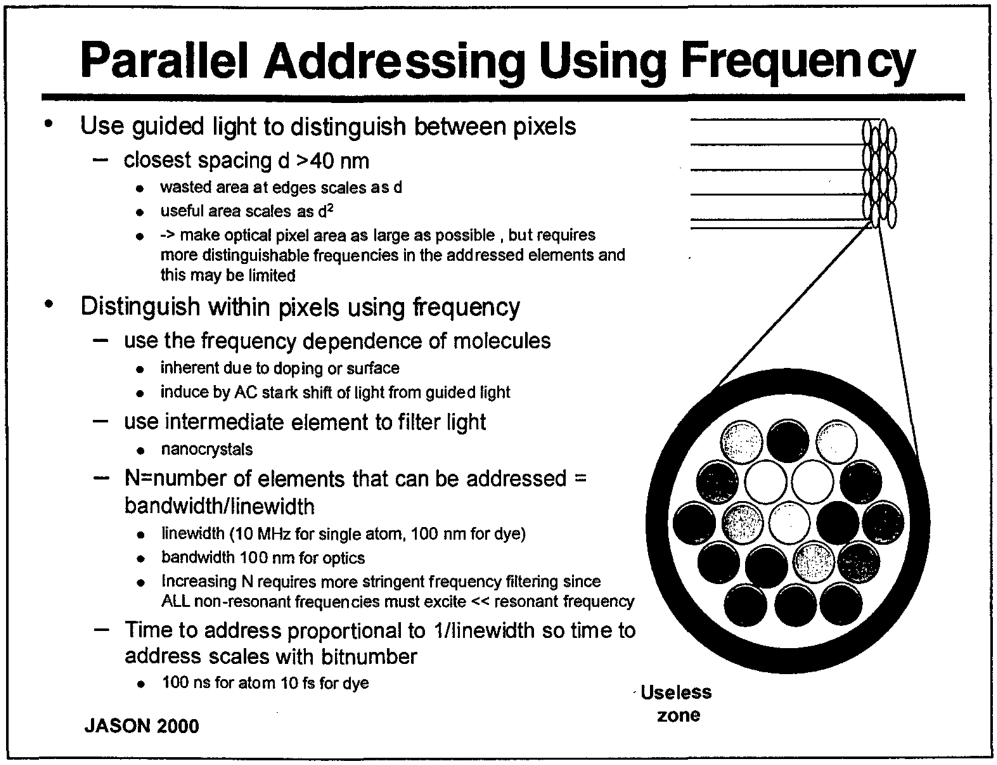
APPENDIX B - Optical Frequency-based Multi-state Addressing

A number of researchers have demonstrated that the fluorescence due to a single molecule can be observed. It is also possible to change the optical or electrical properties of these single molecules. This suggests that one could create devices, such as memories, where each element is composed of a single molecule; however, the input and output of these devices would be optical, and optical devices cannot be closely packed. The probes have been optical near field devices, that must at least fan out to devices in which the light can propagate freely. Assuming an index of refraction of 5 for the light guides, this implies that the light guides must have dimensions of at least $\lambda/10$, where λ is the optical wavelength. For 400 nm light, this gives 40 nm x 40 nm of area even for a device that excites only a single molecule. This is not a large win in area over what is expected to be available in Si.

The free space propagation requirement does not hold if one is willing to address the different memory elements using something other than spatial localization. Consider the 40nmx40nm waveguide discussed above, and divide it into 64 sections 5 nm x 5 nm. One can then flood illuminate the waveguide, so all 64 squares are illuminated, but only one specific resonant molecule will be excited. Thus 64 distinct frequencies would be required to address the material. Some schemes for obtaining such frequencies will be discussed below.

It is important to note that the effective density of the memory will be much lower than the 5 nm x 5 nm suggested above because of the difficulty of separately addressing different 40 nm bins. Even if one assumes a perfect waveguide where the electric field goes to zero at the edge of the



Parallel Addressing Using Frequency

- Use guided light to distinguish between pixels
  - closest spacing d >40 nm
    - wasted area at edges scales as d
    - useful area scales as d^2
    - -> make optical pixel area as large as possible , but requires more distinguishable frequencies in the addressed elements and this may be limited
- Distinguish within pixels using frequency
  - use the frequency dependence of molecules
    - inherent due to doping or surface
    - induce by AC stark shift of light from guided light
  - use intermediate element to filter light
    - nanocrystals
  - N=number of elements that can be addressed = bandwidth/linewidth
    - linewidth (10 MHz for single atom, 100 nm for dye)
    - bandwidth 100 nm for optics
    - Increasing N requires more stringent frequency filtering since ALL non-resonant frequencies must excite << resonant frequency
  - Time to address proportional to 1/linewidth so time to address scales with bitnumber
    - 100 ns for atom 10 fs for dye

Useless zone

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guide, there must be some space between adjacent waveguides to prevent light from one from leaking into the other. In addition, the waveguide light cannot actually address elements at its edge where the electric field is zero. Even if only 10% of the peak height in the waveguide is required to address the element, that still means that there is a deadzone of 0.05 lambda at the edges of the device. If λ in the material is 80nm, this means 4 nm of dead zone around the edge. This eliminates 28 of the possible elements, leaving only 36 of the 64 elements as addressable, which of course also reduces the number of distinct frequencies that are required to address the array. If another 5% of the wavelength is required as a separation between waveguides, this makes only 1/3 of the area usable, which could require increasing the effective bit size from 5 x5 nm to 15x15 nm. This effect can be reduced by using larger area waveguides since the dead area increases linearly with the size of the waveguide, but the usable area increases with the square of the size of the waveguide. Using a larger area waveguide would of course require more distinct frequencies in order to address the bits within the increased area.

There are several techniques that might be used to provide the frequency separation among the bits. One approach would be to tailor the material in each bit by differential doping, for example. An alternate approach would be to exploit the spatial dependence of the light intensity within the waveguide to induce a spatially dependent frequency shift in the material. The AC Stark shift for an atom is of the order of 1 MHz/(mW/cm^2). The area of the waveguide would be 10^{-11} square cm, so 1 microwatt would give a shift that covers the visible spectrum. The frequency shift would of course not be unique to a point, but be spread over regions of equal intensity.

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